Interfacing and set-up of Toshiba T6963C

Introduction

The Toshiba T6963C is a very popular LCD controller for use in small graphics modules. It is capable of controlling displays with a resolution up to 240x128. Because of its low power and small outline it is most suitable for mobile applications such as PDAs, MP3 players or mobile measurement equipment.

A number of Hitachi Liquid Crystal Display modules have this controller built-in these include the SP12N002 & SP14N001. Although this controller is small, it has the capability of displaying and merging text and graphics and it manages all the interfacing signals to the displays Row and Column drivers.

Other related documents:

- Interfacing and set-up of the Sanyo LC7981 controller: Application Note AN-030.
- Driving Displays with T6963C and Touch Panel from a PIC: Application Note AN-037
- Datasheet of T6963C:
  http://www.semicon.toshiba.co.jp/td/en/ASSP/Display_Driver_ICs/en_20030618_T6963C_datasheet.pdf

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1 Basic Operations and Information

1.1 Main Features

- Resolution up to 240x128 pixels or 320x64 pixels
- Capable of displaying text and graphics
- Build-in character generator ROM (CG-ROM) with 128 pre-defined characters
- 8 bit parallel bus and signal lines for interfacing to a micro controller. Data and commands from and to the micro controller are multiplexed on this bus.
- Capable of controlling up to 64 kByte of external display memory. (Hitachi's SP14 & SP12 have 8 kBytes of VRAM)
- Duty Ratio for display multiplex driving in the range of 1/16 up to 1/128
- Current consumption 3-4 mA maximum
- Build-in crystal oscillator
- Operating temperature –20 to +70 degrees Celsius

1.2 Abbreviations and terms in this document

MPU/MCU	**M**icro **P**rocessor/**C**ontroller **U**nit
LCD	**L**iquid **C**rystal **D**isplay
STN	**S**uper **T**wisted **N**ematic – a Liquid Crystal Display technology
SRAM	**S**tatic **R**andom **A**ccess **M**emory (keeps its values as long as voltage is applied).
DRAM	**D**ynamic **R**andom **A**ccess **M**emory (keeps its values just a few microseconds and needs to be refreshed).
CG-ROM	**C**haracter **G**enerator **R**ead **O**nly **M**emory – Non-volatile memory within the T6963C. It contains pre-defined characters which can easily be displayed. A table of them can be found in the T6963C datasheet.
h	The small letter "h" at the end of a number means that this number is in the Hexadecimal Format.
VRAM	Video RAM. Although, this is external memory, it is the RAM for the T6963C and thus, all displaying operations are performed via this RAM.
240x128	Example of a display resolution. The first number indicates the horizontal resolution and the second number the vertical resolution.

Table 1: Abbreviations and terms

1.3 Document Overview

Although the T6963C is a controller for small LCDs, it has a lot of functions and options. This section gives a short overview of the structure of this Application Note. The document is split into the three sections which can be identified in the block diagram below. The first part of the Application Note is about connecting a display to the T6963C. The second part is about connecting and communicating with a micro controller and external display memory. The third part is about the T6963C itself. It describes the options this LCD controller has available and how to set them up.

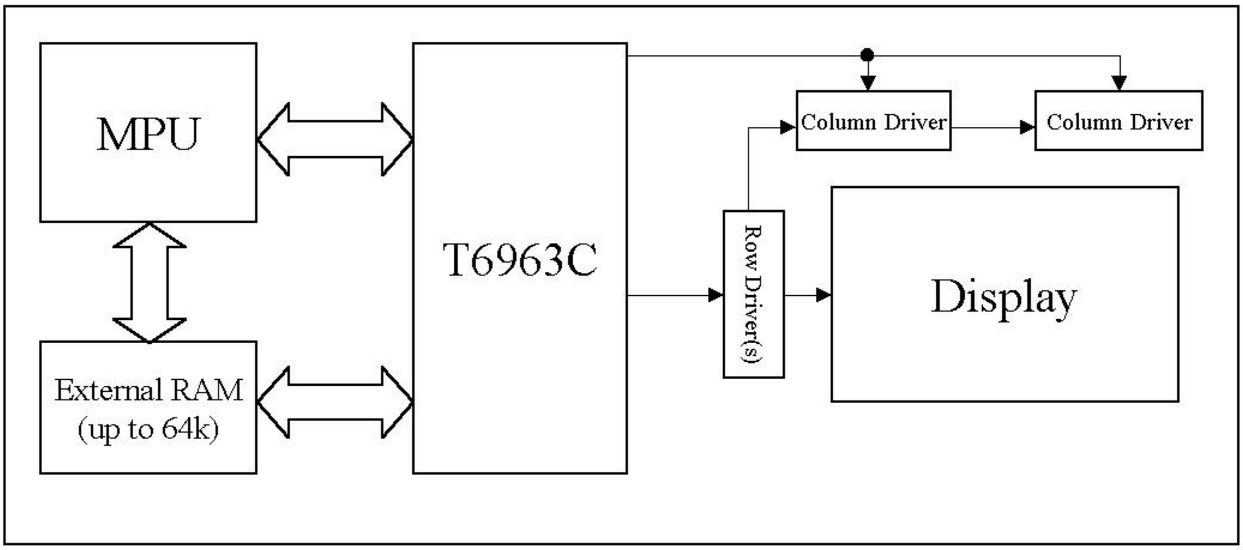

Figure 1: Block diagram of a typical display neighborhood

Of course, the connection to a display and micro controller needs some software code. A brief description of the necessary code can be found in the T6963C section of this document.

Software means, commands from a MPU. The T6963C can not operate without a controlling element (usually a MPU). The T6963C is controlled by commands and data from the MPU. It is not possible, to load instructions or a program into the T6963C itself. Every operation and set-up parameter must be sent by the MPU. Every software consideration or command, mentioned in this Application Note, means a set of commands or data sent by the MPU.

2 Connection to a Display

2.1 Single/Dual Scan

The T6963C is used to control the row and column drivers of monochrome STN graphic displays with a resolution up to 240x128 pixels. The display row and column drivers are connected to the T6963C via a number of timing signals and one or two serial data lines. These signals vary dependent on whether it is a Single Scan display or a Dual Scan display.

Single Scan displays with a resolution of, for example, 240x128 pixels have three column drivers and two row drivers (e.g. column drivers can drive 80 lines and the row drivers 64 lines). Dual Scan displays are separated in an upper and a lower half. A 240x128 display would still have 2 row drivers but 6 column drivers. Three drivers are used for the upper half and three for the lower half of the display. The Dual Scan method is used to increase the contrast on STN displays (The smaller the LCD area (lower duty) the lower driving voltage needs to be to achieve the same contrast as a single scan device). Both the SP12N002 & SP14N001 are single scan devices. Please find more information about active/passive display technologies in Application Note AN-002.

2.2 Timing Signals

2.2.1 Single Scan

/DUAL (Pin 54): This signal must be driven “high” when using a Single Scan display.

/SDSEL (Pin 62): This signal is used to choose the data transmission method to the display row and column drivers. It must be driven “high” when the data is sent by even/odd separation method and “low” when simple serial method is used. The display’s datasheet should give information if this is necessary. (Usually, it is not!)

HOD (51), ED (Pin 52): Serial data signal lines for the column drivers. If /SDSEL is “low” (data sending method is “simple-serial”), all data comes from the ED line. If /SDSEL is driven “high”, (even/odd separation is used), ED provides the data for the even columns and HOD for the odd columns. (On many displays, these signals are just called D0 and D1 or serial data).

HSCP (Pin 53): Shift Clock for serial data. The edge (typically the falling) of this signal causes the current column driver to take one or two (depends on /SDSEL) bits from the data lines in its input latch. (Other names: CL2, CP, Clock, XCK, Shift Clock).

LP (Pin 55): Latch Pulse for column drivers. Shift clock pulse for row drivers. The edge (typically the falling) of this signal causes all column drivers to output the latched signals to the display lines. This edge also causes the current row driver to switch to the next row. The time delay between the output of the column drivers and the switching to the next row is called Horizontal non-display period. (Other names of LP: Horizontal Sync, Load, CL1).

CDATA (Pin 56): Synchronous signal for the row drivers. The edge (typically the falling) of this signal indicates a new frame. The frequency of this signal is called Frame Rate. (Other names: First Line Marker, Frame, Vertical Sync, YD, Line Clock).

FR (Pin 57): This signal must be provided to both, the row and column drivers. They use this signal to change the polarity of the LCD driving voltage to prevent a DC component applied to the Liquid Crystal material. This signal is called M-Signal on most displays. (For details, please see section 4.1.2 Applying Power to the system).

2.2.2 Dual Scan

/DUAL (Pin 54): For a Dual Scan display, this pin must be driven “low”.

/SDSEL (Pin 62): Same as for Single Scan. Drive this signal “low”, when the display data transmission method shall be simple serial. “High” will cause transmission by even/odd separation.

LOD (Pin 49, shared with /ce0), HOD (Pin 51) ED (Pin 52): Serial display data signals. When /SDSEL is “low” (Data transmission by simple serial method), all data to the columns is provided via the ED line. If /SDSEL is “high” (data transmission by even/odd separation), the ED-line provides the data for the even columns in the upper and lower part of the display. HOD provides data for the odd columns in the upper area of the display and LOD provides data for the odd columns in the lower half of the display. On displays, data signal(s) usually are just called “D”, “Data” or “Serial Data”

HSCP (Pin 53), LSCP (Pin 50, shared with /ce1): Shift clocks for serial data. HSCP is for the upper half of the display an LSCP is for the lower area of the display. Function is the same as for Single Scan. The edge (usually the falling) of these signals causes the current column driver to take data bits in its input latch. (Other names: CL2, CP, Clock, XCK, Shift Clock).

LP (Pin 55): Latch Pulse for column driver. Shift clock pulse for row driver. The edge (usually the falling) of this signal causes all column drivers to output the latched signals to the lines. This edge also causes the row drivers to switch to the next row. (Other names: Horizontal Sync, Load, CL1).

CDATA (Pin 56): Synchronous Signal for the row drivers. The edge (typically the falling) of this signal indicates a new frame. This signal is also called First Line Marker and the frequency is called Frame Rate. (Other names: Frame, Vertical Sync, YD, Line Clock).

FR (Pin 57): This signal must be provided to both, the row and column drivers. They use this signal to change the polarity of the LCD driving voltage to prevent a DC component applied to the Liquid Crystal material. On most displays, this signal is called M-Signal. (For details, please see section 4.1.2 Applying Power to the system).

Note: LOD and LSCP are only available when Dual Scan is used. For Single Scan operation, these Pins have the name /ce0 and /ce1 and can be used as chip enable signals for VRAM.

3 Connection to a MPU and Display Memory

Typically, the T6963C is connected to a micro controller unit and external display memory, often called VRAM or display RAM.

3.1 Display Memory – VRAM

3.1.1 Basic Considerations

The T6963C can control up to 64 kByte display memory which must be of SRAM type memory (The T6963C can not refresh DRAM). The T6963C has 16 address lines, 8 data lines and several controlling lines to access the display memory.

An option would be the direct mapping of the display memory in the micro controller internal RAM. The advantage would be easy manipulation of the RAM by the micro controller. (Without external address decoder logic).

The T6963C differs from most other LCD controllers in its use of the display RAM. A fixed area of memory is normally allocated for text, graphics and the external character generator, but with the T6963C the size for each area can be set by software commands. This means that the area for text, graphics and external character generator can be freely allocated within the external memory, up to 64 kByte.

With Dual Scan displays, LCD1 (top half) is allocated in the first half of the VRAM & LCD2 (bottom half) is allocated in the second half of the VRAM but both areas must be allocated identically with respect to text, graphics and the external character generator area. The address line ad15 is used to switch between the memory for the first screen and the second screen.

Note:
In this document, the words “VRAM”, “display memory” and “external RAM” mean the same.

3.1.2 Pins for VRAM Communication

d0~d7 (Pins 22-26 and 28-30)	Data I/O pins for VRAM
ad0~ad15 (Pins 33-48)	Address lines for VRAM
R/W(Pin 31)	Read/Write signal for VRAM
/ce (Pin 32)	Chip Enable pin for VRAM of any address
/ce0 (Pin 49)	Chip Enable pin for VRAM in the address range 0000h to 07FFh
/ce1 (Pin 50)	Chip Enable pin for VRAM in the address range 0800h to 0FFFh

Table 2: Pins for memory communications

Notes

1. /ce0 and /ce1 are only available for Single Scan display mode. In Dual Scan display mode, these pins become timing signals for the lower half of the display.
2. The display memory address line ad15 selects the display memory for the lower and upper half of a Dual Scan display. Drive this pin "low" to access the upper half and drive it "high" for the lower half.

3.2 MPU Connection

3.2.1 General Considerations

The communication between the T6963C and a MPU is not complex and there are only few hardware considerations. The T6963C has an 8 bit data bus and several signals for communication with a MPU. (See a list of pins in Table 3: Pins for MPU communication).

For the interface timing, please see the T6963C datasheet. Note, if the MPU instruction execution time is less than 200 ns, wait states, NOPs or delay loops may be required to allow time for the T6963C to recognise the instruction.

3.2.2 Pins for MPU Communication

D0~D7 (Pins 10-17)	Data I/O pins for communications between MPU and T6963C.
/WR (Pin 18)	Data Write. It must be driven "low" to write data to VRAM via the T6963C.
/RD (Pin 19)	Data Read. It must be driven "low" to read data from VRAM via the T6963C.
/CE (Pin 20)	Chip Enable. It must be driven "low" while MPU communicates with T6963C.
C/D (Pin 21)	Command/Write selection. To write or read data, it must be driven "low". To write a Command or read status, it must be driven "high".

Table 3: Pins for MPU communications

4 Setting up the T6963C

With the above information, it will be possible to connect the T6963C pins to the correct display pins. If using the SP12N002 or SP14N001 these connections are already made. If using another display please check the displays datasheet for considerations such as Single/Dual Scan, simple serial or even/odd separation and of course duty cycle and resolution.

The T6963C must be set-up so that it operates correctly with the given display characteristics. There are both, hardware and software issues to consider. Hardware issues include selecting the correct pins which determine the size of the display (i.e. the resolution) or set the Font Size for example. Software issues include commands from the micro controller for example to set the "software" size of the display (please see next sections for details).

4.1 General Hardware Considerations of the T6963C

4.1.1 General Pins

V_{DD} (Pins 27,61) V_{SS} (Pin 63)	Power connection. +5 V and Ground. Depending on the power supply, it may be necessary to add some capacitors as close as possible to filter noise and ripple.
/HALT (Pin 1)	Driving it "low" stops the clock oscillation and a reset is issued. Check datasheet for register states after reset.
/RESET (Pin 2)	Driving it "low" causes a reset and the T6963C is initialised. Check datasheet for register states after reset. This pin has an internal pull-up.
DSPON (Pin 50)	Control output pin for external DC/DC. DSPON is "low" when /HALT or /RESET are driven "low". This is useful to switch the display off while T6963C is not in normal operation.
XI (Pin 66)	External clock source input.
XO (Pin 67)	External clock source output.
CH1 (Pin 58), CH2 (Pin 59)	Check signal outputs.
/T1 (Pin 65), /T2 (Pin 64)	Test inputs. Leave them open.

Table 4: Pins with general functions

4.1.2 Applying Power to the system

After powering on the whole system, a reset of the T6963C should be issued to ensure correct operation. This is achieved by holding the /RESET pin “low” for at least 5-6 clock cycles. V_{DD} must be stable at +5 V for the reset. This can be achieved with an output pin of the MCU or just with a simple capacitor/resistor network. See Figure 2 for an example.

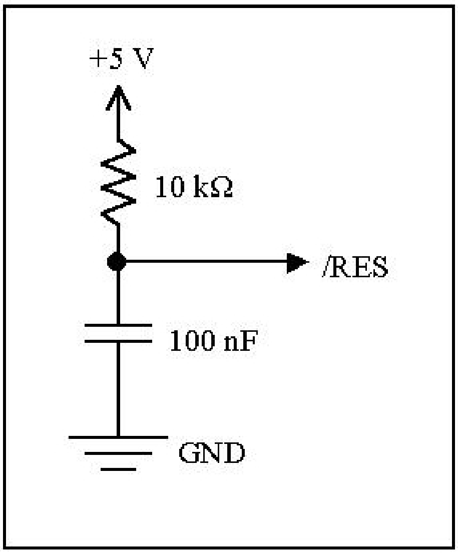

Figure 2: Example for Reset circuit

It is important to keep the correct power on sequence for the whole system because the T6963C generates the M-Signal (In the T6963C datasheet it is called FR-Signal) for the LCD row and column drivers. The M-Signal is used to change the polarity of the driving voltage so that in sum, no DC is applied to the Liquid Crystal material. To ensure the stability of the M-Signal, the T6963C must be fully initialised before applying the Voltage V_{EE} to the Liquid Crystal material. The displays /DISPOFF pin can be useful for this purpose.

If T6963C is reset during normal operation, it must be ensured that the V_{EE} voltage and the display are turned off until the T6963C is fully reinitialised. This applies also when using the /HALT pin to stop the T6963C operation. (/HALT includes a reset). The DSPON pin (pin 60) of the T6963C can be useful for controlling the power supply to the display. This pin is an output and indicates if the T6963C /HALT or /RESET Pin is “low”. (DSPON is then “low”, too).

The correct power up sequence would be:

1. Apply power to MPU and T6963C. The display and the display's power (V_{EE}) should be off.
2. Reset T6963C and wait until it is fully initialised. (5-6 clock cycles).
3. Apply power to the display (V_{EE} on), for example with the T6963C DSPON pin
4. Apply signals to the display and switch it on (for example with the /DISPOFF pin of the display).
5. Normal operating parameters are reached.

Notes
1. The states of the T6963C registers after a "reset" or "halt" are in the T6963C datasheet.
2. For powering off, the reverse applies, i.e. first, switch off the display, remove signals, remove V_{EE} display power and then switch off the MPU and T6963C (with proper delays, too).

4.2 Hardware considerations for setting up the T6963C for a display

4.2.1 Pins

The states of the following pins are used to set the T6963C for a particular display:

/DUAL (Pin 54): For Dual Scan displays, this pin must be driven "low". However, the most displays are Single Scan and this pin can be set "high".

/SDSEL (Pin 62): This pin must be driven "high" when the data is sent by even/odd separation method. However, most of the displays use the simple serial method and therefore this pin can be driven "low".

MDS, MD0, MD1 (Pins 3, 4, 5): Pins for selection of LCD vertical size. Please see the T6963C datasheet for valid values. For example the combination MDS:MD1:MD0 = H:L:L would set 128 vertical dots (for a Single Scan display).

MD2, MD3 (Pins 6, 7): Pins used to select the number of columns. Columns in this instance refers to the number of displayable characters per row. There can be 4 combinations: 32 columns, 40 columns, 64 columns and 80 columns. Please find more information about this setting in the following section.

FS0, FS1 (Pins 8, 9): Pins for selection of Font Size. There are four Font Sizes available: 5x8, 6x8, 7x8 and 8x8 dots per font. (horizontal dots by vertical dots). The horizontal Font Size does not affect the driving signals, i.e. it does not change the horizontal resolution of the display when changing the Font Size. Please find more information about Font Size in the following section.

4.2.2 Font Size, Number of Columns and Pixels per Column

The T6963C datasheet is unclear regarding to horizontal resolution, Font Size, the number of columns and the pixel width of one column. The T6963C data sheet says that the number of columns can be chosen by driving the pins MD2 and MD3 but it is not specific about how many horizontal pixels are in one column and additionally the selectable options with the MD2 and MD3 pins are poor. (Only four display sizes). The datasheet does not specify the maximum horizontal resolution this controller can drive.

In combination with the Font Size one might have expected that the formula “Font Size” multiplied with the “MD2 and MD3 column setting” must result in the actual horizontal display resolution. But in practice, changing the Font Size does not affect any driving signals and therefore the Font Size does not set anything regarding the horizontal display resolution. The most important “task” for the Font Size is the character spacing and that the mapping of display pixels to VRAM bits becomes clear and logical. For further details please see section 4.3.3 Memory and Font Size.

The actual “physical” display resolution is determined by software commands. The state on the MD2 and MD3 pins should be selected that the number of horizontal pixels is a multiple of the number of columns. For 240 horizontal pixels a number of columns of 40 is recommended.

4.3 Software for controlling a display

Various functions and options can be selected using software commands. The commands are sent from the micro controller and affect the display, the external memory and the T6963C functions.

4.3.1 General Considerations about Commands and Data

When sending commands and/or data to the T6963C a certain sequence must be obeyed. First of all, before sending any commands and/or data to the T6963C, a status check must be performed. The status check is necessary to find out, if the T6963C is ready to accept any commands and/or data. The status check is done by driving /RD “low” (and of course, /WD “high”), /CE “low” and C/D “high”. Now, a status byte can be read from the data lines D7~D0. Each bit (except bit 5) represents a certain state of the T6963C. Please check the datasheet for details. Important for the status check in normal mode are bits 0 and 1 of the status byte (STA0 and STA1, D0 is LSB). The T6963C is still busy when one of them is “low”. To accept commands and/or data STA0 and STA1 must be “high”.

After a successful status check, the T6963C is ready to accept commands and/or data. A command is always one byte long. However, some commands, for example the command “Set Cursor Pointer”, requires some data (this example would need two data bytes, the X-coordinate and the Y-coordinate). There are commands which need two data bytes, one data byte or none. The data must be sent before the Command, i.e. if a command needs two data bytes, the first data byte must be sent, then the next and finally the actual command. (status checks must be performed before sending each byte).

4.3.2 Commands to set the Display Size

As mentioned in previous sections, the actual display size is set using software commands. These commands come under the heading of “Set Control Word”.

Two commands “Set Text Area” and “Set Graphic Area” are important to set the “software” display size. Both commands need one data byte. Their values (in HEX) indicate how many bytes are used for one complete row, i.e. how “far” it is from one byte to the same byte of the next row. It makes sense to assign the same value to both Text Area and Graphics Area. See the section “4.3.3 Memory and Font Size” for more details about how many bytes of memory are used for one row.

The two other commands of “Set Control Word” are “Set Text Home Address” and “Set Graphic Home Address”. They are used to set the beginning of the text area and graphic area in the VRAM. The text and graphic area can be freely allocated but of course, care should be taken that they do not overlap. Please find an example of memory allocation below and a summary of the command in Table 5.

Value (HEX)	**Function**	**Data Byte 1**	**Data Byte 2**
0100 0011 (43h)	Set Graphic Area	Number of Columns	Nothing
0100 0001 (41h)	Set Text Area	Number of Columns	Nothing
0100 0010 (42h)	Set Graphic Home Address	Low Byte	High Byte
0100 0000 (40h)	Set Text Home Address	Low Byte	High Byte

Table 5: Overview of Command "Set Control Word"

This Figure is an example for the memory allocation in the VRAM.

The graphics area and text area are big enough to store data to fill several pages of a display. (For a 240x128 display, 3840 bytes are necessary to fill one screen with graphics).

This can be useful to implement for example a scrolling function. Scrolling can be done for example by altering the Text Home Address.

The small space between the areas is for safety but usually not required. It should just show that the areas can really be free allocated.

The external character generator area is always 2 kByte and can only be set to certain addresses. For details, please see section “4.3.6 Character Generator”

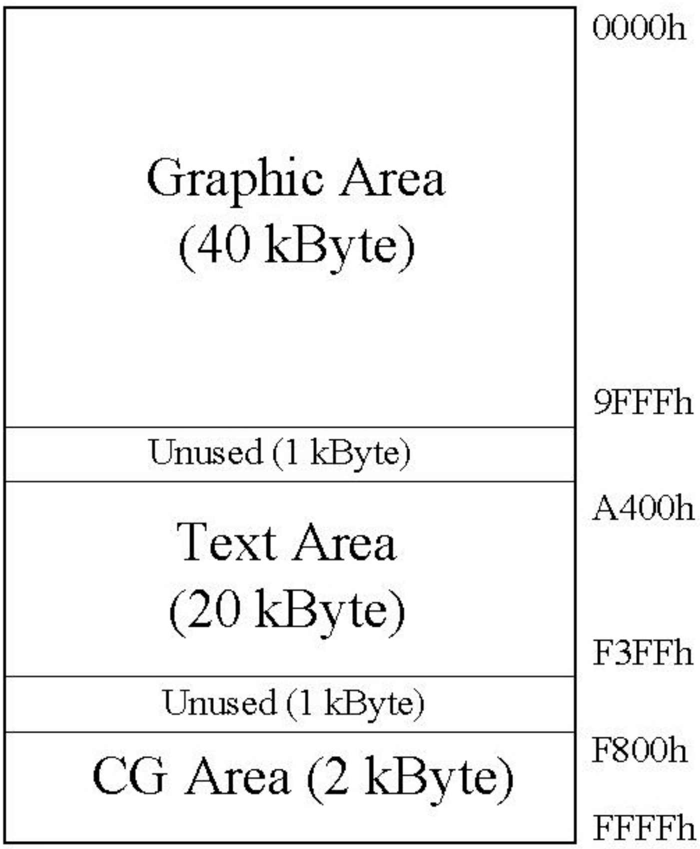

Figure 3: Example of Memory allocation

4.3.3 Memory and Font Size

Although the Font Size is selected by hardware pins, it is necessary to talk about it here in the software section. The Font Size affects the number of bits used of a byte for displaying text and graphics. If the font is 8 horizontal pixels wide, every bit of a byte in the VRAM controls a pixel on the display. If the Font Size is 6 horizontal pixels wide, only 6 bits of each byte control pixels. The first two bits are then “don’t care”. That means, regardless of its size, a character is controlled by one byte in memory, always. Keep this in mind for setting the Text and Graphic Areas (see previous section).

Example: With a Font Size of 6x8 and 40 columns, one row needs 40 bytes of memory and a total of 10 bytes are “don’t care”. With a font of 8x8 and 30 columns, 30 bytes of memory are necessary for one row. (Here with no “don’t cares”).

Again, it does not matter if text or graphics are used, the Font Size affects both. This should be kept in mind when choosing the number of columns and calculating the required memory space for applications.

4.3.4 “Mode Set” Commands from 80h to 8Fh

The information given in the T6963C datasheet is not clear about this set of commands. With these commands, the user can set two functions. The first is how graphics and text are merged on the display. The second enables/disables functions such as “Cursor on/off”, “Text on/off” etc. These commands require no data byte.

The graphics/text merge function is set by the Command values 80h to 8Fh:

Binary Code	Hex Code (internal CG)	Hex Code (external CG)	Function
1000 X000	80h	88h	OR Mode
1000 X001	81h	89h	EXOR Mode
1000 X011	83h	8Bh	AND Mode
1000 X100	84h	8Ch	Text Attribute Mode

Table 6: The “Mode Set” Commands from 80h to 8Fh

Note:
Bit 3 (“X”) is used to set the character generator. Bit 3 = “0” means “Internal CG-ROM Mode” and Bit 3 = “1” means “External CG-RAM Mode”.

OR Mode: In the OR-Mode, text and graphics can be displayed and the data is logically “OR-ed”. This is the most common way of combining text and graphics for example labels on buttons.

EXOR-Mode: In this mode, the text and graphics data is combined via the logical “exclusive OR”. This can be useful to display text in negative mode, i.e. white text on black background.

AND-Mode: The text and graphic data shown on the display are combined via the logical “AND function”.

TEXT ATTRIBUTE: This option is only available when displaying just text. The Text Attribute values are stored in the graphic area of the display memory, which was defined by the "Set Graphic Home Address" command. Because the graphic memory is also used both text and graphic display bits must be enabled with the "Mode Set" commands (values 90h to 9Fh, see next section). The TEXT ATTRIBUTE options are "Reverse display" (show the character in negative mode, i.e. white character on black background), "Character Blink" and "Inhibit" (do not display this character).

Notes

1. When choosing a certain mode, it applies for the whole display. It is for example not possible to apply attributes to text in one part of the display and graphics in another part of the display.
2. There are no other bit combinations for the "Mode Set" commands in the range of 80h to 8Fh than the four shown above in Table 6.

4.3.5 The "Mode Set" Commands from 90h to 9Fh

The second set of commands are selected with bit combinations 90h to 9Fh. 9h means binary 1001. The second nibble bit combinations set the cursor and text and/or graphics display:

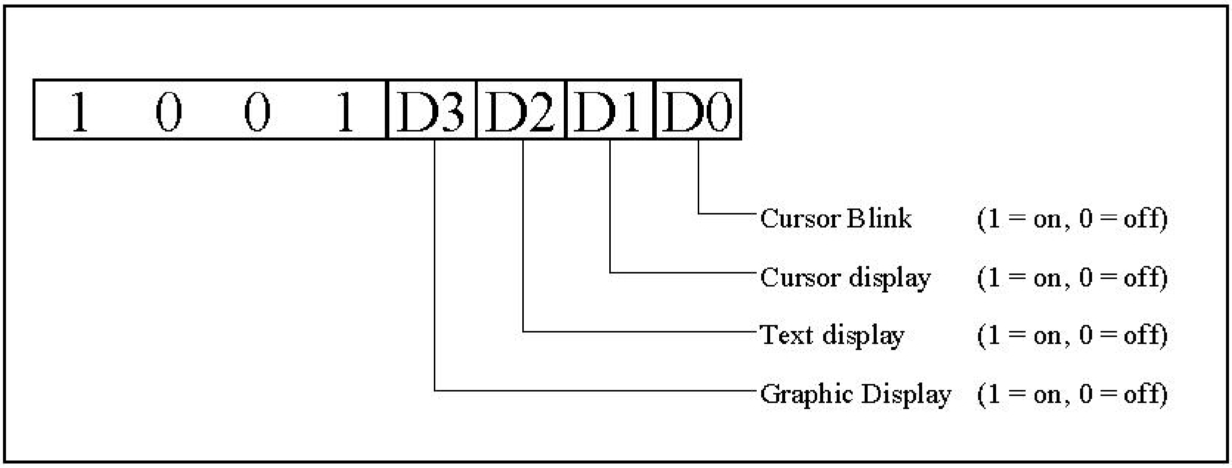

Figure 4: Combinations for "Mode Set" (Functions from 90h to 9Fh)

The four least significant bits can be configured for "Display Off" (all "0") to "Text On, Graphic On". Nearly any combinations are possible. See the T6963C datasheet for details.

4.3.6 Character Generator

The T6963C has the capability to generate characters in two ways. The first way is with the built-in character generator ROM. It contains 128 pre-defined characters. The second way is using the external character generator.

To ensure high flexibility, the T6963C can operate in two modes. One mode is using the internal character generator ROM for the 128 pre-defined characters and the external character generator area for 128 user-defined characters. The other mode is using only the external character generator RAM for up to 256 user-defined characters. The two modes are called “Internal CG-ROM Mode” and “External CG-RAM Mode”. (The configuration is selected by the “Mode Set” commands. See previous section).

The location of external CG-Area in VRAM is set by the command “Set Offset Register”. The external CG-Area is always 2 kByte in size (2048 Bytes) and can store up to 256 user-defined characters. (Each character needs 8 bytes, 256 x 8 bytes = 2048 bytes). The command “Set Offset Register” is 22h (0010 0010) and needs 2 bytes of data. (The second data byte of the Command “Set Offset Register” must always be 00h)

The five least significant bits of the first data byte sets the 2k external CG-Area within VRAM. With five bits, 32 different memory segments can be selected ($2^5 = 32$). (There are 32 possible locations for a block of 2 kBytes within 64 kBytes of memory therefore 5 bits are enough to set the external CG-RAM area). The 5 bit combination corresponds to a memory block address in the table below.

Least significant data bits of first data byte	**CG-Area (start and end), 2 kByte**
00000	0000h – 07FFh
00001	0800h – 0FFFh
00010	1000h – 17FFh
…..	…..
11101	E800h – EFFFh
11110	F000h – F7FFh
11111	F800h – FFFFh

Table 7: Possible external character generator areas

In “Internal CG-ROM Mode” the first 1024 bytes (1024 = 400h) of the external character generator memory block are not used therefore the address of the first external character must have an offset of 400h to the start address (With a start address of 1000h for example the first character would be located at 1400h).

In “internal CG-ROM mode”, the character codes 00h to 7Fh are used for selecting a character from the internal character generator ROM. The codes 80h to FFh are used for the external character generator RAM. In the mode “External CG-RAM Mode”, the internal character generator is disabled and all character codes (00h to FFh) represent characters in the external CG-RAM.

Each character in the external RAM is 8 bytes wide (A character can have a Font Size of up to 8 by 8 dots) and therefore the character with code 80h is located from 1400h to 1407h. (And therefore the data for this character must be written to these addresses. See the example in section 5). To show this character on the display, "Text Mode" must be enabled (By the "Mode Set" Commands, see previous section) the selected character is taken from the memory location in character RAM and stored in the TEXT area of VRAM prior to display on the screen. The address pointer must be set to the appropriate address in the Text Area of VRAM and then, the command "Write Data" must be executed with the data byte "80h". The T6963C knows automatically this is a character from the external CG-RAM and writes all 8 bytes from the CG-RAM locations 1400h to 1407h to the appropriate text memory location.

Note:
A table of the internal character generator ROM content is on page 26 in the T6963C datasheet. A character code of 7Fh represents the letter "f" for the common CG-ROM type 0101. This character generator table is similar to a small area of the ASCII Table. The characters of the T6963C CG-ROM from 00h to 5Fh are the same as for ASCII 20h to 7Fh. The ASCII characters have an offset of 20h compared to the T6963C characters. If you want an ASCII character displayed, you need its hex code and subtract 20h. If you send this value as character code to the T6963C you have it. To see an ASCII table visit www.asciitable.com

Below is a table describing how the T6963C combines the Off Set Register value and character code to locate the physical memory location of the chosen character.

<table>
<tr><td>RAM Address (HEX)</td><td colspan="4">1h</td><td colspan="4">4h</td><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>VRAM Address (Binary)</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Actual Meaning</td><td colspan="5">5 Bits Offset Register Data (0 0010 = 02h)</td><td colspan="8">8 Bits Character Code (1000 0000 = 80h)</td><td colspan="3">3 Bits Line Scan</td></tr>
</table>

Table 8: Dependence of CG-RAM area and character code

4.3.7 Address Pointer Considerations

The T6963C address pointer has several functions. Basically, it is used to set the address in the VRAM where to read or to write data. The address pointer is set by the “Set Address Pointer” command 24h and needs two data bytes a low address byte and a high address byte. (The addresses in the VRAM are 16 Bits wide).

To write data from the MPU into the VRAM, the address pointer has to be set to the required address and a “Write Data” or “Auto Write Data” command executed.

To read data from the VRAM, set the address pointer and execute a “Read Data” or “Auto Read Data” command.

The “Write/Read Data” commands can be executed so that the address pointer is increased or decreased automatically. An “Auto Write/Read Data” command controls the increase of the address pointer.

To show data on the display, set the address pointer to the appropriate address in the Text or Graphic Area in the VRAM, enable the display with the “Mode Set” commands and execute a “Write Data” Command. The data now stored in the VRAM area is shown automatically on the display.

Example: To show a 16 dot line in the upper left corner of the display (as a graphic): (Assumed that Text Home Address is set to 0000h, Graphic Home Address to 0200h, Graphic is enabled & the Font Size is set to 8 by 8. Do not forget: Font Size affects both, Text and Graphics!)

1. Set Address Pointer to 0200h
2. Execute “Write Data” Command (with increase of Address Pointer) with the data byte FFh
3. Execute “Write Data” Command with the data byte FFh

Note: Do a status check before sending a command or data.

4.3.8 Additional Commands

The T6963C has many more commands, there is a complete overview of these additional Commands in the datasheet.

5 Example of external Character Generation

This section gives an example how the external character generator can be used to display the Euro (€) symbol. The Euro symbol is not in the pre-defined character set of the internal character generator ROM but with the introduction of the Euro currency in many countries in the European Union, it can be helpful for a display controller to have the capability of showing it. This example shows how the Euro symbol is stored in the external character generator RAM as a user-defined character and how it can be displayed. Be careful, the status checks are not mentioned.

Before the external character generator RAM can be used, its area in the VRAM must be set. This is set with the command “Set Offset Register”. Let’s set the character generator RAM location to E000h to E7FFh. As explained in the datasheet, the last 5 bits of the Offset register data byte must be 11100 to achieve this. The internal character generator is also being used therefore only the second half of the external character generator memory block can be used.

Execute command “Set Offset Register” with the data bytes 1Ch (000 11100) and 00h. (The character with code 80h is then located at the address E400h – 1110 0100 0000 0000).

After the setting of the CG-RAM area, the character data can be written. The Euro symbol is constructed as shown below:

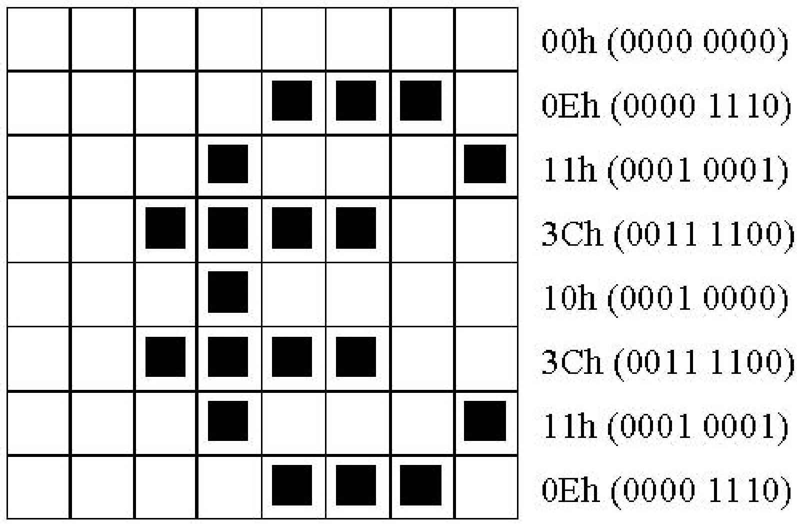

Figure 5: Euro Symbol as "Dot Character"

To write the data into the CG-RAM, the address pointer must be set to the appropriate address. Assuming that the Euro symbol is the first character we wish to store it will have the character code 80h, the address pointer must therefore be set to E400h. After setting the address pointer, the data can be written with the commands “Write Data” or “Auto Write Data”. Do not forget the proper status checks.

To show the Euro symbol on the display, set the address pointer to an address in the Text Area of the VRAM and execute the command “Write Data” with the data byte 80h. (Text Mode must be enabled). The T6963C automatically knows that this is a character from the external character generator RAM.

6 Summary

This Application Note wants to cover the issues where the T6963C datasheet is not clear or even wrong, for example the Font Size and column width relationship. It is important that the Font Size according to the Text Area and Graphics Area, which determine the bit-to-pixel mapping of the VRAM-to-Display.

The actual horizontal "software resolution" of the display is set with the "Set Control Word" commands. These commands determine how many bytes make one row and therefore how to determine the VRAM address of the start of the next row. Check this value, if the display shows either no characters at the end of a row (no wrap or wrap too late) or characters double (wrap too early).

Another thing to consider is the start address of the external character generator. This is set by the "Set Offset Register" command. The CG-Area is 2 kByte and therefore 5 Bits are sufficient to set it in a 64 kByte memory. ($2^5 = 32$). These five bits are the least significant bits of the first data byte of the command.

Most important thing: Don't panic! Do not let the datasheet of the T6963C or this Application Note confuse you. The datasheet is not always clear. However, when reading it several times, it becomes more logical. Try also looking for code examples for the T6963C. The code in the datasheet is written for a Z80 micro controller and can be helpful although initially confusing. Be aware that the code contains some errors!

Please see application note AN-037 Interfacing displays with T6963C & Touch Panel from a PIC for further code examples and explanations.

Cautions

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