DATA SHEET

SBN6400G

64-COMMON Driver for Dot-Matrix STN LCD

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1 GENERAL

1.1 Description

The SBN6400G is a 64-COMMON driver, designed to be paired with the SBN0064G 64-SEGMENT driver to drive a dot-matrix STN LCD panel.

Functionally, the SBN6400G includes 64 COMMON drivers, on-chip RC oscillator, a 64-bit bi-directional shift register, and timing generation circuit. The RC oscillator needs only an external resistor and capacitor. The timing generation circuit generates clocks and display control signals for both the SBN6400G and the SBN0064G.

To expand COMMON number, the SBN6400G can be cascaded in master-slave connection.

1.2 Features

- To be paired with the SBN0064G 64-SEGMENT driver.
- 64-COMMON STN LCD drivers.
- Master Mode and Slave Mode for cascaded connection to expand COMMON numbers.
- On-chip RC oscillator; only an external resistor and an external capacitor are needed.
- Provides clocks and display control signal to the SBN0064G.
- External LCD bias (V0, V1, V4, V5).
- Selectable display duty cycle: 1/48, 1/64, 1/96, 1/128.
- Operating voltage range (V_{DD}): 2.7 ~ 5.5 volts.
- LCD bias voltage (V_{LCD}=V_{DD} - V5, the voltage added to the LCD cell): 13 volts (max).
- Negative power supply (V_{NEG}=V_{DD}-V_{EE}): 16 volts (max).
- Operating frequency range: 550 KHz.
- Operating temperature range: -20 to +75 °C.
- Storage temperature range: -55 to +125 °C.

1.3 Ordering information

Table 1 Ordering information

PRODUCT TYPE	DESCRIPTION
SBN6400G-LQFPG	LQFP100 Pb-free package.
SBN6400G-QFPG	QFP100 Pb-free package.
SBN6400G-LQFP	LQFP100 general package.
SBN6400G-QFP	QFP100 general package.
SBN6400G-D	tested die.

2 FUNCTIONAL BLOCK DIAGRAM AND DESCRIPTION

2.1 Functional block diagram

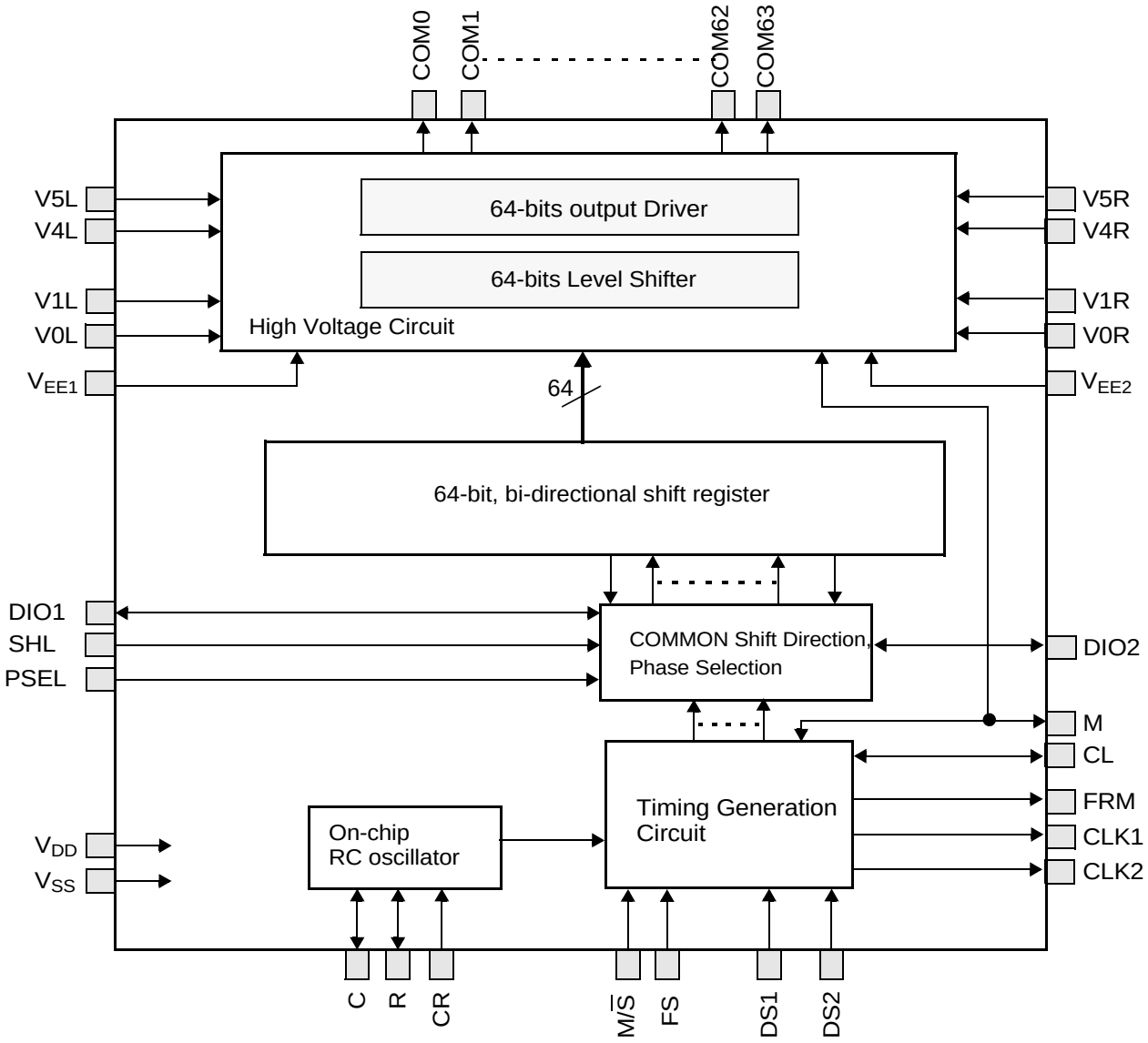


Fig.1 Functional Block Diagram

3 PIN(PAD) ASSIGNMENT, PAD COORDINATES, SIGNAL DESCRIPTION

3.1 The SBN6400G pinning diagram (LQFP100 or QFP100)

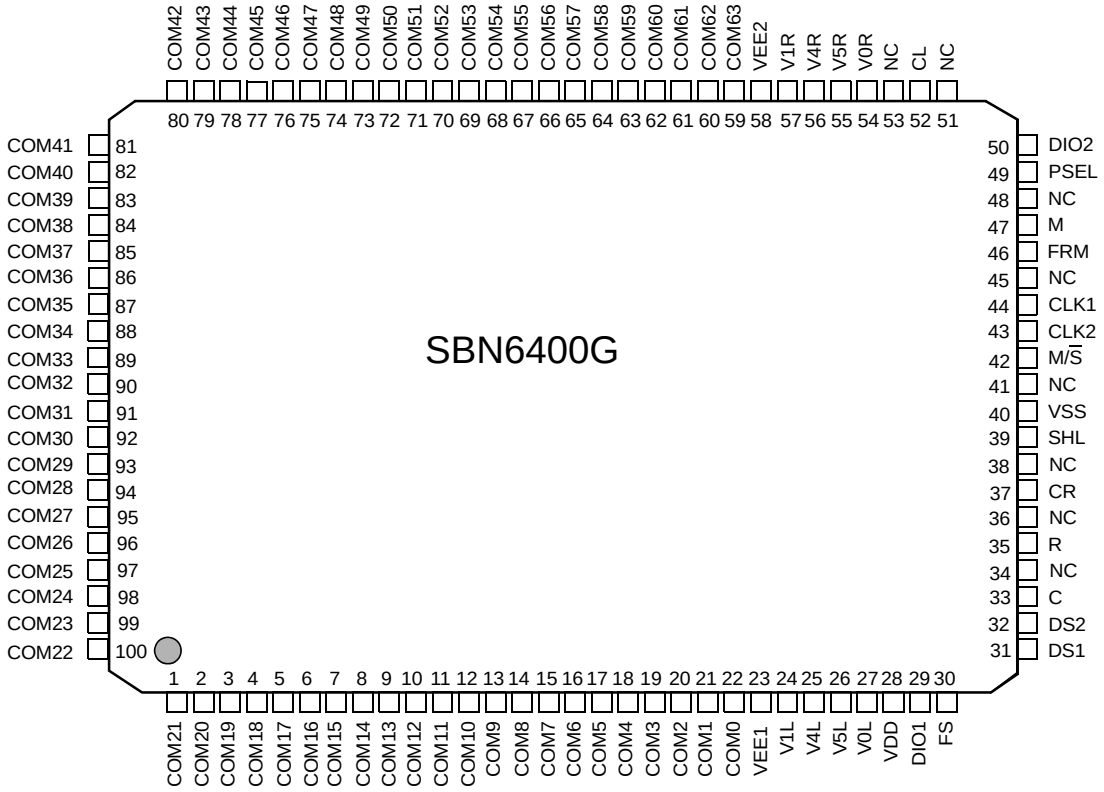
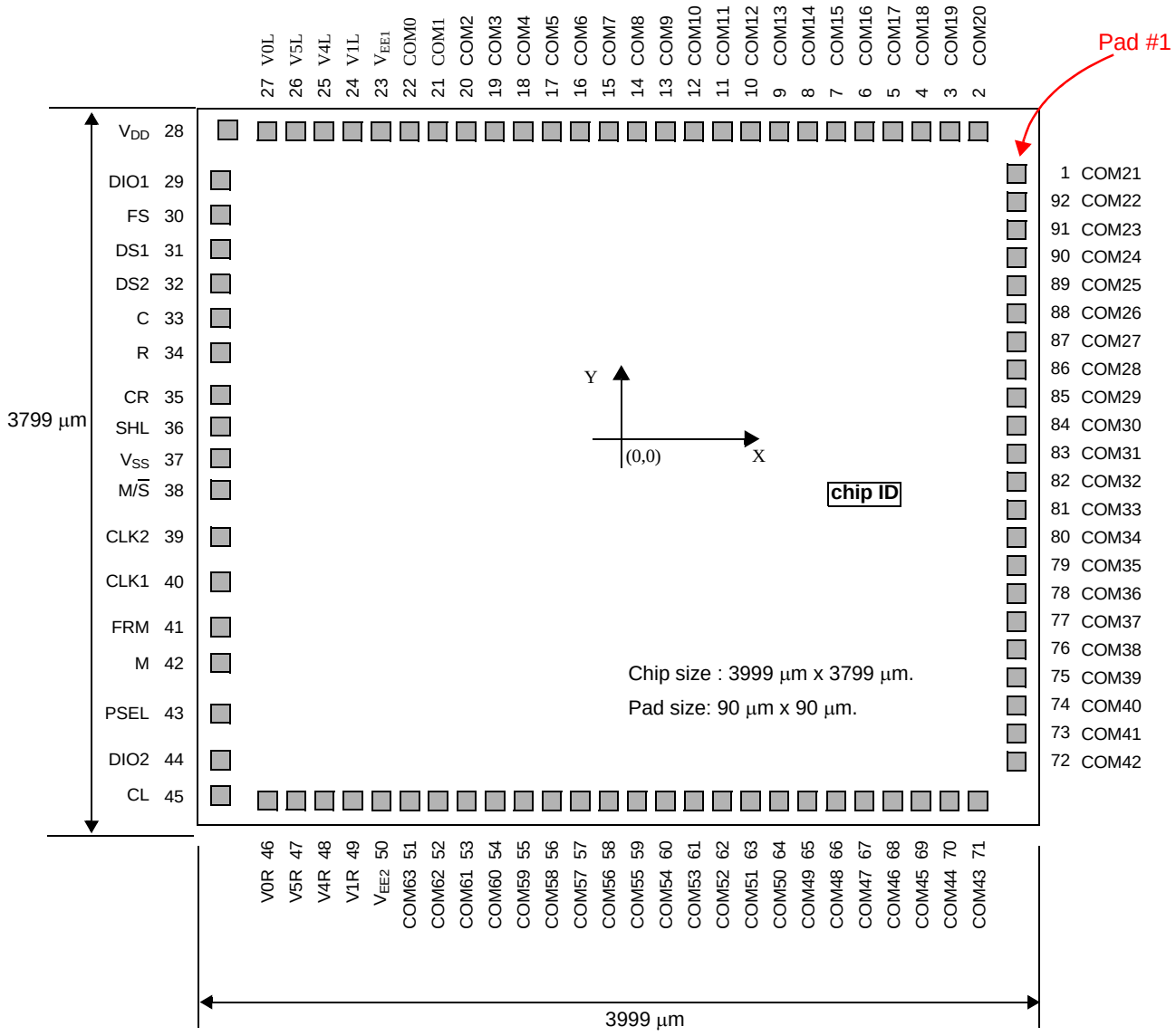


Fig.2 Pin assignment of LQFP100/QFP100 package.

3.2 The SBN6400G pad placement



Note:

(1) The total of pad number is 92.

(2) The chip ID is located at the right middle part of the chip.

(3) The chip ID is 12001.

(4) The die origin is at the center of the chip.

(5) For chip_on_board bonding, **chip carrier** should be connected to VDD or left open. **Chip carrier** is the metal pad to which the die is attached.

Fig.3 The pad placement

3.3 Pad coordinates

Table 2 The pad coordinates (unit: μm)

PAD NO.	PAD NAME	X	Y
1	COM21	1866	1575
2	COM20	1659	1768
3	COM19	1529	1768
4	COM18	1399	1768
5	COM17	1269	1768
6	COM16	1139	1768
7	COM15	1009	1768
8	COM14	879	1768
9	COM13	749	1768
10	COM12	619	1768
11	COM11	489	1768
12	COM10	359	1768
13	COM9	229	1768
14	COM8	99	1768
15	COM7	-31	1768
16	COM6	-161	1768
17	COM5	-291	1768
18	COM4	-421	1768
19	COM3	-551	1768
20	COM2	-681	1768
21	COM1	-811	1768
22	COM0	-941	1768
23	V_{EE1}	-1071	1768
24	V1L	-1201	1768
25	V4L	-1331	1768
26	V5L	-1461	1768
27	V0L	-1591	1768
28	V_{DD}	-1838	1785
29	DIO1	-1857	1533
30	FS	-1857	1345
31	DS1	-1857	1165
32	DS2	-1857	984
33	C	-1857	776
34	R	-1852	601

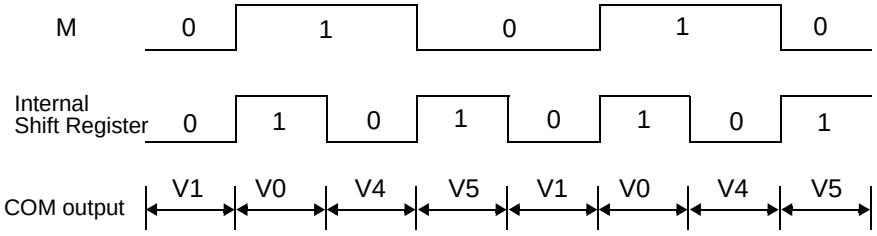
PAD NO.	PAD NAME	X	Y
35	CR	-1857	305
36	SHL	-1857	163
37	V_{SS}	-1857	20
38	M/$\overline{S}$	-1857	-130
39	CLK2	-1857	-379
40	CLK1	-1857	-625
41	FRM	-1857	-873
42	M	-1857	-1052
43	PSEL	-1857	-1276
44	DIO2	-1857	-1558
45	CL	-1857	-1748
46	V0R	-1591	-1767
47	V5R	-1461	-1767
48	V4R	-1331	-1767
49	V1R	-1201	-1767
50	V_{EE2}	-1071	-1767
51	COM63	-941	-1767
52	COM62	-811	-1767
53	COM61	-681	-1767
54	COM60	-551	-1767
55	COM59	-421	-1767
56	COM58	-291	-1767
57	COM57	-161	-1767
58	COM56	-31	-1767
59	COM55	99	-1767
60	COM54	229	-1767
61	COM53	359	-1767
62	COM52	489	-1767
63	COM51	619	-1767
64	COM50	749	-1767
65	COM49	879	-1767
66	COM48	1009	-1767
67	COM47	1139	-1767
68	COM46	1269	-1767

PAD NO.	PAD NAME	X	Y
69	COM45	1399	-1767
70	COM44	1529	-1767
71	COM43	1659	-1767
72	COM42	1866	-1575
73	COM41	1866	-1425
74	COM40	1866	-1275
75	COM39	1866	-1125
76	COM38	1866	-974
77	COM37	1866	-824
78	COM36	1866	-674
79	COM35	1866	-524
80	COM34	1866	-374
81	COM33	1866	-224
82	COM32	1866	-74
83	COM31	1866	76
84	COM30	1866	226
85	COM29	1866	376
86	COM28	1866	525
87	COM27	1866	675
88	COM26	1866	825
89	COM25	1866	975
90	COM24	1866	1125
91	COM23	1866	1275
92	COM22	1866	1425

3.4 Signal description

Table 3 Pin signal description

To avoid a latch-up effect at power-on: V_{SS} – 0.5 V < voltage at any pin at any time < V_{DD} + 0.5 V .

Pin number	Pad number	SYMBOL	DESCRIPTION
1~22, 59~100	1~22, 51~92	COM21~0 COM63~22	COMMON outputs. The output voltage level of COMMON outputs are decided by the combination of the alternating frame signal (M) and the internal Shift Register Output. Depending on the value of M and the Shift Register Output, a single voltage level is selected from V0, V1, V4, or V5 for COMMON driver, as shown in Fig. 4.  Fig.4 COMMON output voltage level
23, 58	23, 50	V_{EE1}, V_{EE2}	External negative power supply for LCD bias. These two inputs are internally connected together inside the chip. However, to avoid flickering, same external negative bias voltage should be connected to these two inputs.
24, 25, 26, 27	24, 25, 26, 27	V1L, V4L, V5L V0L	External LCD Bias voltage. These pins should be connected to V1, V4, V5, and V_{DD}, respectively, of the external LCD bias circuit, and the condition VDD≥V1≥V2≥V3≥V4≥V5 must always be met. These pins are internally connected to V1R, V4R, V5R, and V0R, respectively.
28	28	V_{DD}	Power supply for logic circuit of the chip. The V_{DD} should be in the range from 2.7 volts to 5.5 volts.
29, 50	29, 44	DIO1, DIO2	Input or output for master/slave mode operation in a cascading connection. Please refer to Sections 4.6 and 4.7.
30	30	FS	Oscillator Frequency Selection. When the device operates in master mode, FS is used to select the RC oscillator frequency to make frame frequency approximately equal to 70Hz. If the RC oscillator frequency is 550K Hz (at V_{DD}=5 volts), then this input should be connected to V_{DD}. If the RC oscillator frequency is 225K Hz (at V_{DD}=5 volts), then this input should be connected to V_{SS}. Usually, 550K Hz is recommended and this pin should be connected to V_{DD}. When the device operates in slave mode, this input should be connected to V_{DD}.

Pin number	Pad number	SYMBOL	DESCRIPTION
31, 32	31, 32	DS1, DS2	Display duty selection inputs. These two inputs are used to select display duty cycle when the SBN6400G operates in master mode. These pins are not valid in slave mode and should be connected to V_{DD}.
33, 35, 37	33, 34, 35	C, R, CR	Pins of the on-chip RC oscillator for connection to external resistor and capacitor. When operating in slave mode, the device's C and R terminals should be left open and its CR terminal should be connected to V_{DD}. Instead of the RC oscillator, if an external clock source is to be used, then this clock source should be added to the CR terminal. In this case, both the C and R terminals should be left open.
39	36	SHL	This input is used to select COMMON output sequence When SHL=1, COMMON output sequence is from COM0 to COM63. When SHL=0, COMMON output sequence is from COM63 to COM0.
40	37	V_{SS}	Ground.
42	38	M/$\overline{S}$	This input is used to select Master Mode or Slave Mode. When this input is connected to V_{DD}, the SBN6400G operates in Master Mode. When this input is connected to V_{SS}, the SBN6400G operates in Slave Mode.
43, 44	39, 40	CLK2, CLK1	Clock outputs to the SBN0064G. The frequency of these two clocks is a half of the RC oscillator clock frequency.
46	41	FRM	Frame signal, indicating the start of a frame. When the SBN6400G operates in master mode, its FRM output should be connected to the FRM input of the SBN0064G. When the SBN6400G operates in slave mode, its FRM output should be left open. For the timing of this signal, please refer to Fig. 11
47	42	M	Alternating frame signal for generating LCD biases of reverse polarites. This is an I/O terminal. When the SBN6400G operates in master mode, this terminal becomes output and should be connected to its slave. When the device operates in slave mode, this terminal becomes input and accepts M output from its master.
49	43	PSEL	Phase selection for COMMON output. This input selects the phase relation between the COMMON outputs and the CL clock. If PSEL=1 (i.e., connected to V_{DD}), each COMMON output starts on the rising edge of CL. If PSEL=0 (i.e., connected to V_{SS}), each COMMON output starts on the falling edge of CL. Usually, PSEL should be connected to V_{DD}.

Pin number	Pad number	SYMBOL	DESCRIPTION
52	45	CL	Shift clock for the internal 64-bit, bi-directional shift register. The time duration of each COMMON output is equal to one clock period of the CL clock.
54, 55, 56, 57	46, 47, 48, 49	V0R, V5R, V4R, V1R	External LCD Bias voltage. These terminals should be connected to V1, V4, V5, and V_{DD}, respectively, of the external LCD bias circuit, and the condition VDD≥V1≥V2≥V3≥V4≥V5 must always be met. These terminals are internally connected to V1L, V4L, V5L, and V0L, respectively.
34, 36, 38, 41, 45, 48, 51, 53		NC	No Connection. For package type, these pins should be left open. For die, there is no NC pad.

4 FUNCTIONAL DESCRIPTION

4.1 On-chip RC oscillator

When operating in master mode, the SBN6400G's on-chip RC-type oscillator is used to provide clocks and necessary control signals to itself, its slave, and the SBN0064G SEGMENT Driver.

External resistor R_f and capacitor C_f need to be connected across R, CR, and C, as shown in Fig. 5. The recommended value for R_f is 33K ohm and that for C_f is 20 pF. During PCB layout, the resistor and the capacitor should be placed as close to the SBN6400G as possible, such that stray capacitance, inductance, and resistance can be minimized.

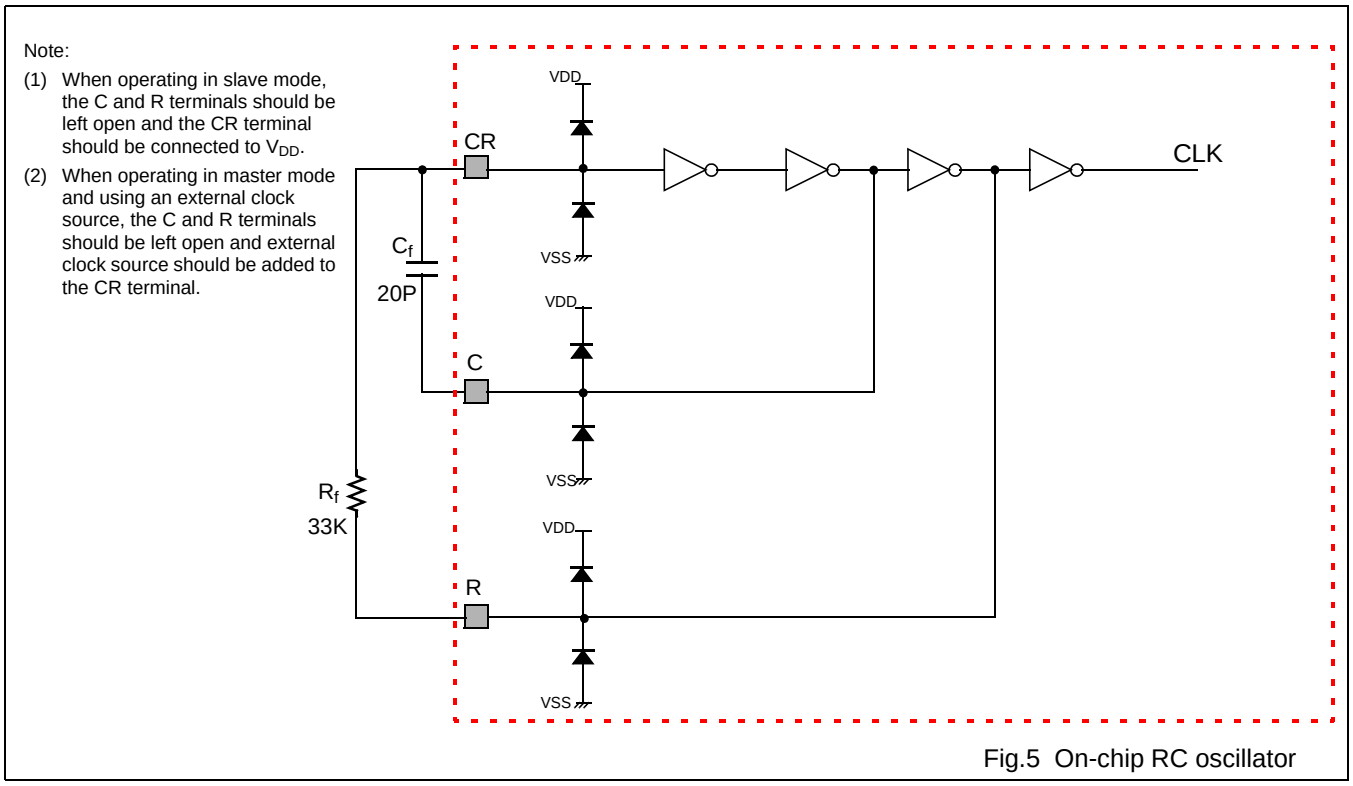


Fig.5 On-chip RC oscillator

The typical oscillation frequency of the oscillator at different power supply voltages, with C_f fixed to 20 pF, is given in Table 4.

Table 4 On-chip RC oscillator characteristics, C_f= 20 pF, T_{amb} = −20 to +75 °C

R_f value (unit: ohm)	VDD=5V	VDD=3V	VDD=2.7V	unit
47K	406	361	350	KHz
43K	443	392	377	
39K	484	425	406	
33K	557	485	463	
30K	601	521	497	

Note:

1. The values given in this table are typical values. ±10% variation from lot to lot may exists.

4.2 RC-oscillator Frequency Selection (FS)

When the RC oscillator frequency is 550 KHz, FS should be connected to V_{DD}. When the RC oscillator frequency is below 300 KHz, FS should be connected to V_{SS}. In the both cases, the purpose of this input is to make frame frequency approximately equal to 70 Hz.

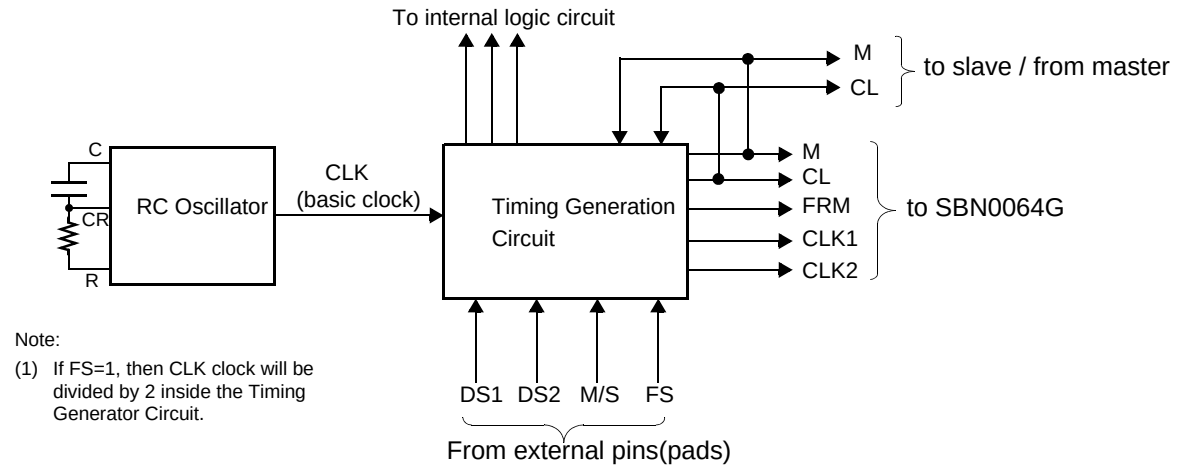
Usually, 550 KHz operation is recommended.

4.3 Timing Generation

The SBN6400G's internal timing generation circuit is shown in Fig. 6.

When M/$\overline{S}$=1, the SBN6400G operates in Master Mode, sends M and CL to its slave, and sends M, CL, FRM, CLK1, and CLK2 to the SBN0064G.

When M/$\overline{S}$=0, the SBN6400G operates in Slave Mode and receives M and CL from its master. In addition, when operating in slave mode, the SBN6400G will not send out FRM, CLK1, and CLK2. These terminals should be left open.



Note:

(1) If FS=1, then CLK clock will be divided by 2 inside the Timing Generator Circuit.

Fig.6 Timing generation circuit

4.4 Duty selection

When the SBN6400G operates in Master Mode, the display duty is decided by its DS1 and DS2 inputs. When the SBN6400G operates in slave mode, its DS1 and DS2 has no function and should be connected to V_{DD}.

Table 5 gives the setting of the DS1 and DS2 and the corresponding display duty cycle.

Table 5 Duty selection

DS1	DS2	Duty
1	1	1/128
1	0	1/96
0	1	1/64
0	0	1/48

4.5 Phase relation between CL and COMMON outputs

The PSEL input is used to select the phase relation between CL clock and COMMON outputs. The CL clock is the shift clock to the internal 64-bit, bi-directional Shift Register. A CL clock period is the time duration for displaying a horizontal line of LCD pixels.

If PSEL=H, the COM0 starts from the rising edge of CL clock. If PSEL=L, then COM0 starts from the falling edge of CL, as shown in Fig. 7.

Usually, it is recommended that PSEL be connected to V_{DD}.

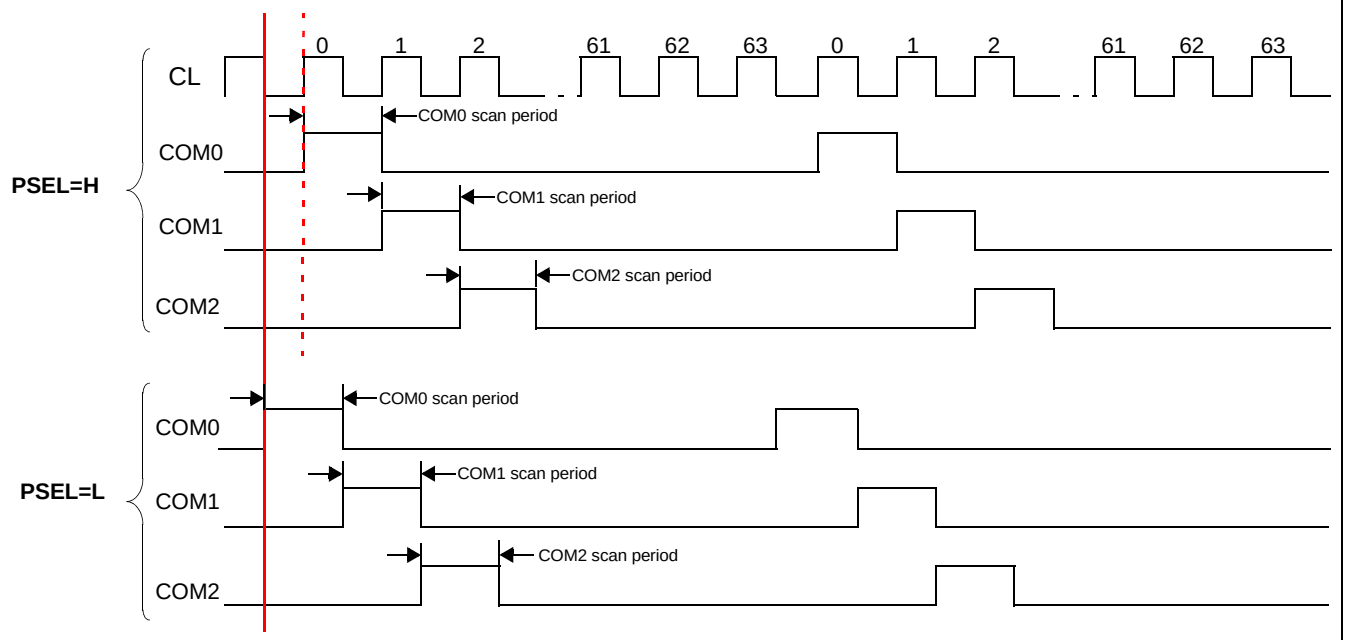


Fig.7 Phase relation between COMMON and CL, as decided by PSEL

4.6 Master/Slave connection

The SBN6400G can be cascaded in master-slave connection to expand the total number of COMMONs.

When a device is selected as master, its DIO1, DIO2, M, and CL are all in output state. Its M output and CL output should be connected to its slave and its M, CL, FRM, CLK1 and CLK2 should be connected to the SBN0064G.

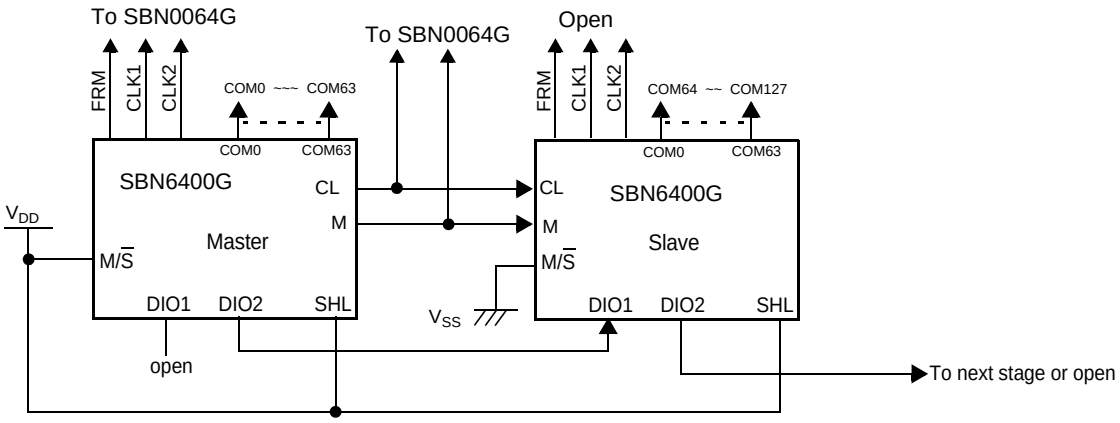


Fig.8 Master/Slave connection with SHL=1

4.7 COMMON output sequence

The COMMON output sequence is decided by both the M/$\overline{S}$ and the SHL inputs, as shown in Table 6.

Table 6 COMMON output sequence in master-slave connection

M/$\overline{S}$	SHL	DIO1	DIO2	COMMON SHIFT DIRECTION	NOTES
1 (master)	1	x	Output	C0 → C63	Note 1
	0	Output	x	C63 → C0	
0 (slave)	1	Input	Output	C0 → C63(master), C0 → C63(slave)	Note 2
	0	Output	Input	C63 → C0(master), C63 → C0(slave)	Note 3

Notes

1. When the SBN6400G is in master mode, both its DIO1 and DIO2 are always output, and COMMON output sequence is decided by SHL. If SHL=1, COM0 is output first and COM63 is output last. If SHL=0, COM63 is output first and COM0 is output last.
2. When the SBN6400G operates in slave mode and its SHL is HIGH, its DIO1 becomes input and its DIO2 becomes output. The slave's DIO1 should be connected to DIO2 of the master. The COM0 of the master is output first. After COM63 of the master is output, COM0 of the slave is output. COM63 of the slave is output last.
3. When the SBN6400G operates in slave mode and its SHL is LOW, its DIO1 becomes output and its DIO2 becomes input. The slave's DIO2 should be connected to DIO1 of the master. The COM63 of the master is output first. After COM0 of the master is output, COM63 of the slave is output. COM0 of the slave is output last.

5 LCD BIAS AND COMMON OUTPUT VOLTAGE

5.1 LCD bias circuit

A typical LCD bias circuit for 1/64 display duty is shown in Fig. 9. The condition $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ must always be met. The maximum allowed voltage for LCD bias (V_{DD}-V_5) is 13 volts. Note that V0 should be connected to V_{DD}.

COMPONENT	RECOMMENDED VALUE
C	0.1 μF, electrolytic
R1	2.2K ohm
R2	10K ohm
R3	10K ohm, variable resistor

Note:

(1) V0 should always be connected to V_{DD}.

(2) For cascading application, it is recommended that a buffer be added for each of V1, V2, V3, V4, and V5. For 64 COM x 64 SEG application, these buffers are not needed.

(3) The LCD bias voltage (V_{LCD} = V0 - V5) should not exceed 13 volts, without regard to display duty.

(4) ***The voltage difference between V_{DD} (the most positve power) and V_{EE} (the most negative power), V_{DD} - V_{EE}, should not exceeds 16 volts, without regards to display duty.***

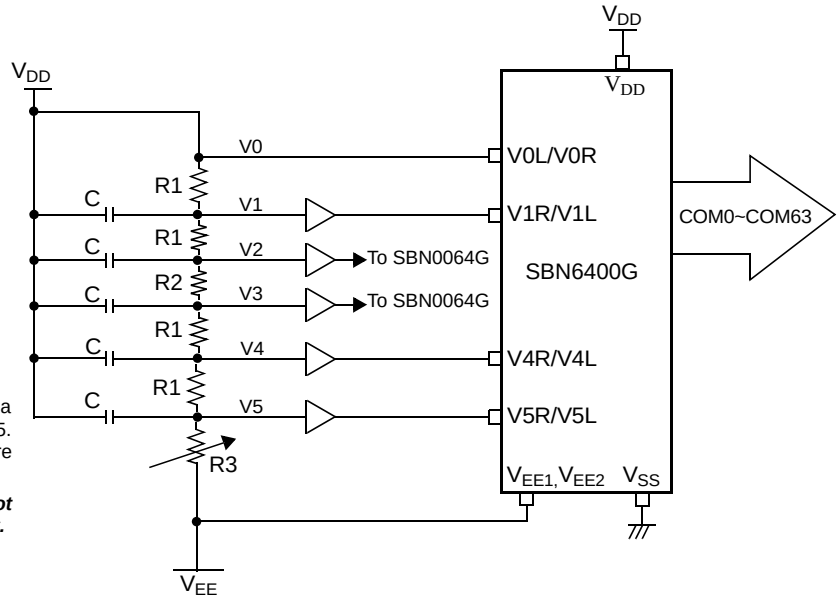


Fig.9 LCD Bias circuit for 1/64 display duty

5.2 Relation of display duty, CL period, LCD bias, and recommended resistor ladder for bias

Table 7gives the relation of display duty, CL period, LCD bias, and recommended resistor ladder for bias.

Table 7 Relation of display duty and LCD bias

Duty	CL period	Bias	Resistor ladder
1/48	64 x CLK2	1/8	R2= 4 x R1
1/64	48 x CLK2	1/9	R2= 5 x R1
1/96	32 x CLK2	1/11	R2= 7 x R1
1/128	24 x CLK2	1/12	R2= 8 x R1

Note:

1. When the display duty cycle 1/64 is chosen, the condition $(R1)/(4 \times R1 + R2) = 1/9$ should be met. We choose R1=2.2K ohm and, therefore, the calculated value of R2 is 11K ohm. As 11K ohm is not a standard value for resistors, we choose a 10K ohm resistor for R1.
2. The duration (period) of a CL clock is a multiple of the CLK2 clock. The time duration of each COMMON output is equal to one period of the CL clock.

5.3 COMMON, SEGMENT output voltage

Table 8 gives the output voltage level of the SBN6400G COMMON Driver and the SBN0064G SEGMENT Driver.

The COMMON output voltage level of the SBN6400G COMMON Driver is decided by the combination of the alternating LCD bias voltage (M) and its internal Shift Register Output.

The SEGMENT output voltage level of the SBN0064G SEGMENT driver is decided by the combination of the alternating LCD bias voltage (M) and the output of its on-chip Display Data Memory.

Table 8 COMMON/SEGMENT output voltage level

Frame (M)	Data/COM	DISPLAY ON/OFF	SEG0~SEG63 (SBN0064G)	COM0~COM63 (SBN6400G)
L	L	ON	V2	V1
L	H	ON	V0	V5
H	L	ON	V3	V4
H	H	ON	V5	V0
x(don't care)	x(don't care)	OFF	V2, V3	x

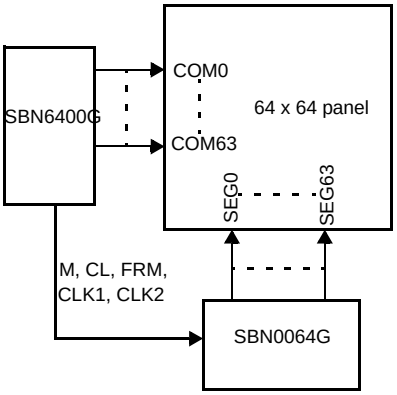
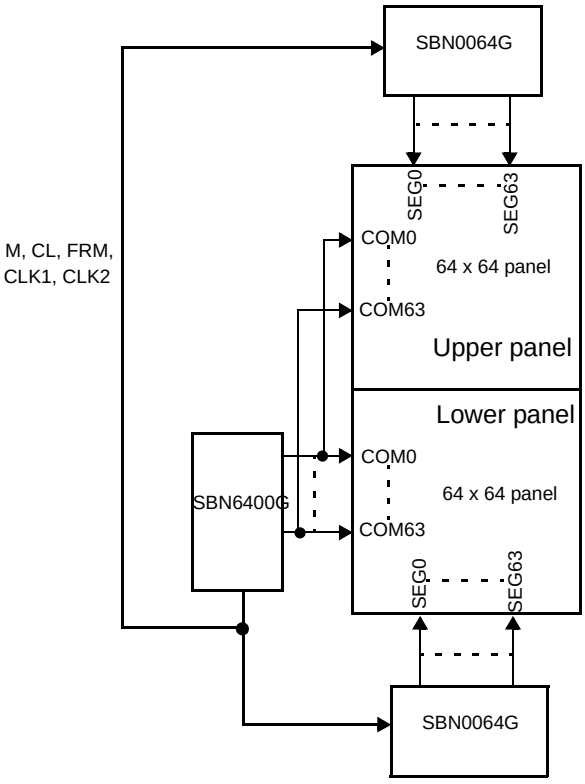
Note:

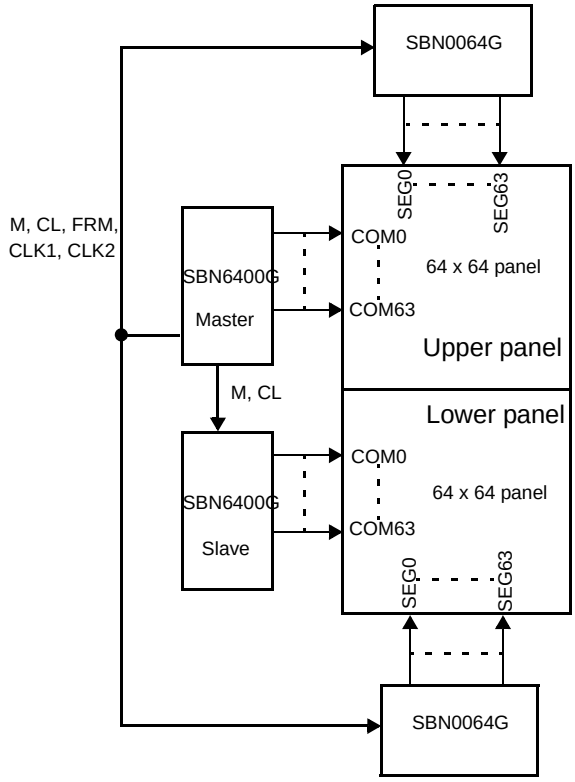
1. "Data" in the "Data/COM" column means the data output from the on-chips Display Data RAM of the SBN0064G SEGMENT Driver, and "COM" means the output of the SBN6400G's internal Shift Register Output, which sequentially activates COM0~COM63.
2. The column DISPLAY ON/OFF is applicable only to the SBN0064G.

6 SYSTEM CONFIGURATION WITH THE SBN0064G

Table 9 gives examples of system configuration with the SBN0064G.

Table 9 Examples of system configuration with the SBN0064G.

Configuration	Description
	One SBN6400G drives the COM 0 ~ 63 of the panel and supplies timing and display control signals M, CL, FRM, CLK1, and CLK2 to one SBN0064G, which interfaces with a host microcontroller and drives SEG 0 ~ 63.
	One SBN6400G drives the COM 0 ~ 63 of both the upper panel and the lower panel, and supplies timing and display control signals M, CL, FRM, CLK1, and CLK2 to two SBN0064G. The two SBN0064G respectively interfaces with the host microcontroller and drives SEG 0 ~ 63 of the upper panel and the lower panel.

Configuration	Description
	One SBN6400G operates in Master Mode and supplies timing and display control signals to two SBN0064G. One SBN6400G operates in Slave Mode and receives M and CL signals from the Master.

7 APPLICATION EXAMPLE 1: MASTER MODE, 1/64 DISPLAY DUTY

7.1 Application circuit for 1/64 display duty, Master Mode operation

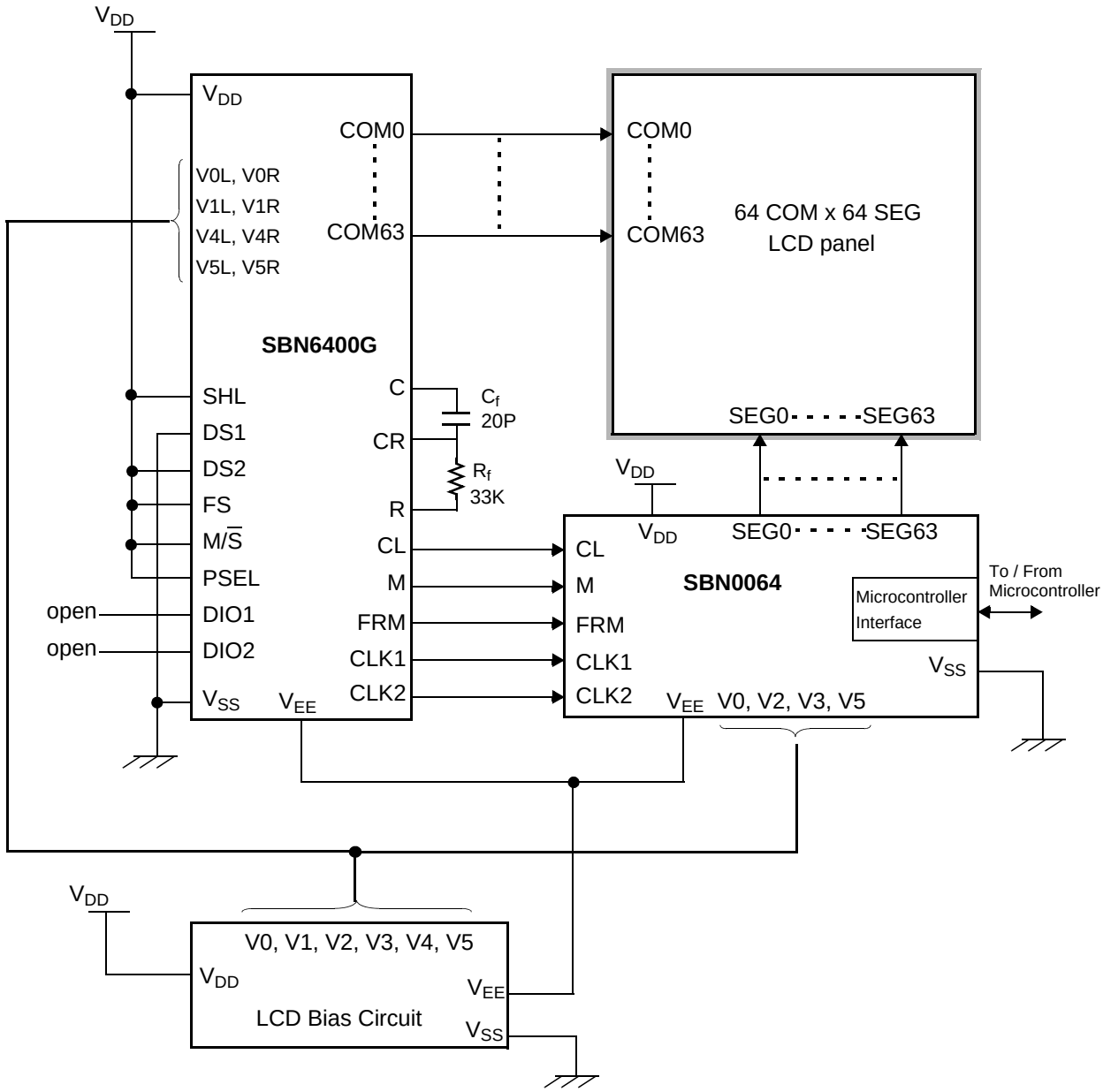


Fig.10 Application circuit for 1/64 display duty, Master Mode operation

7.2 Timing diagram of Master Mode, 1/64 display duty cycle(DS1=L, DS2=H, SHL=H(L), PSEL=H)

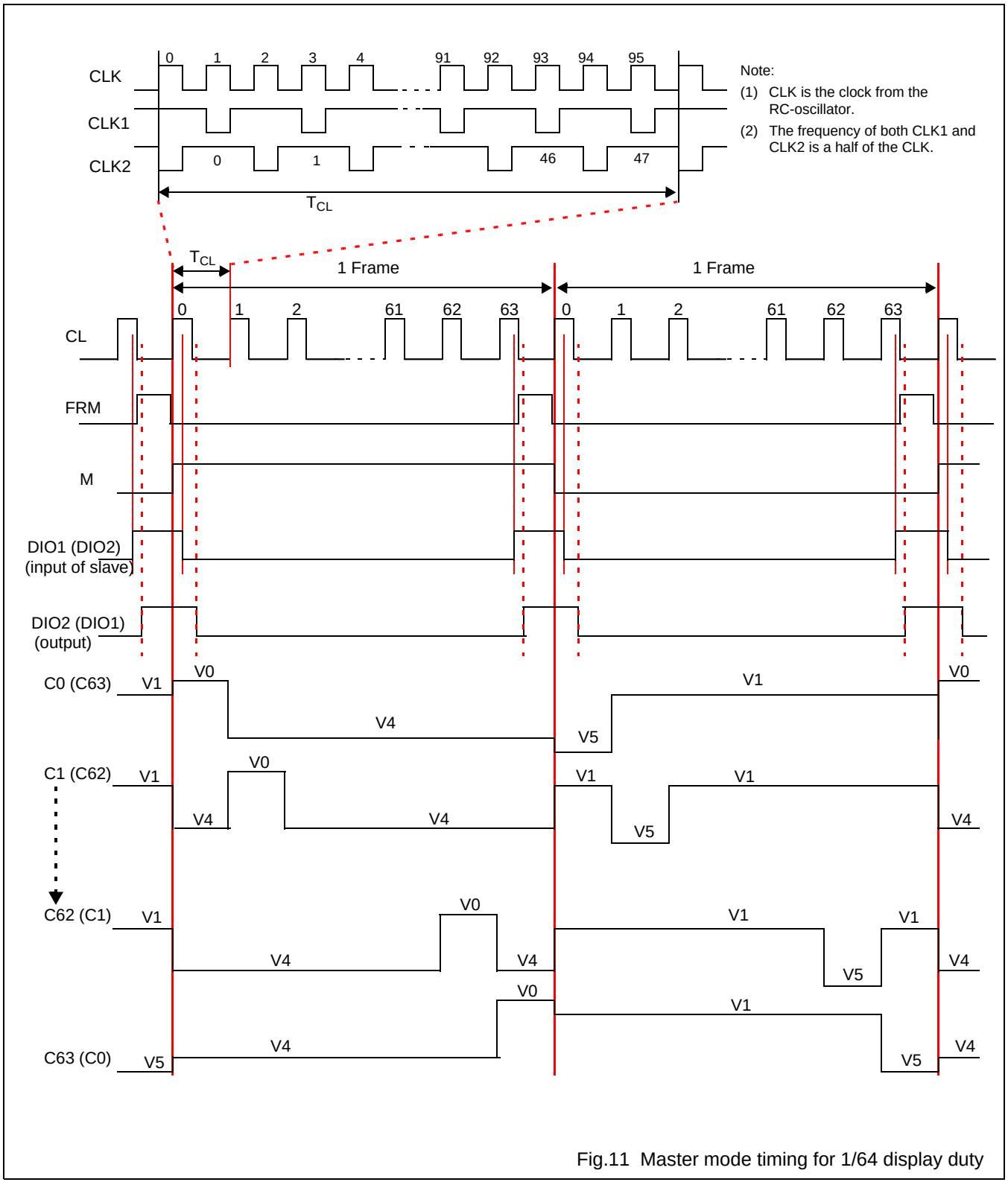


Fig.11 Master mode timing for 1/64 display duty

8 APPLICATION EXAMPLE 2: MASTER MODE, 1/128 DISPLAY DUTY

8.1 Application circuit for 1/128 display duty, Master Mode operation

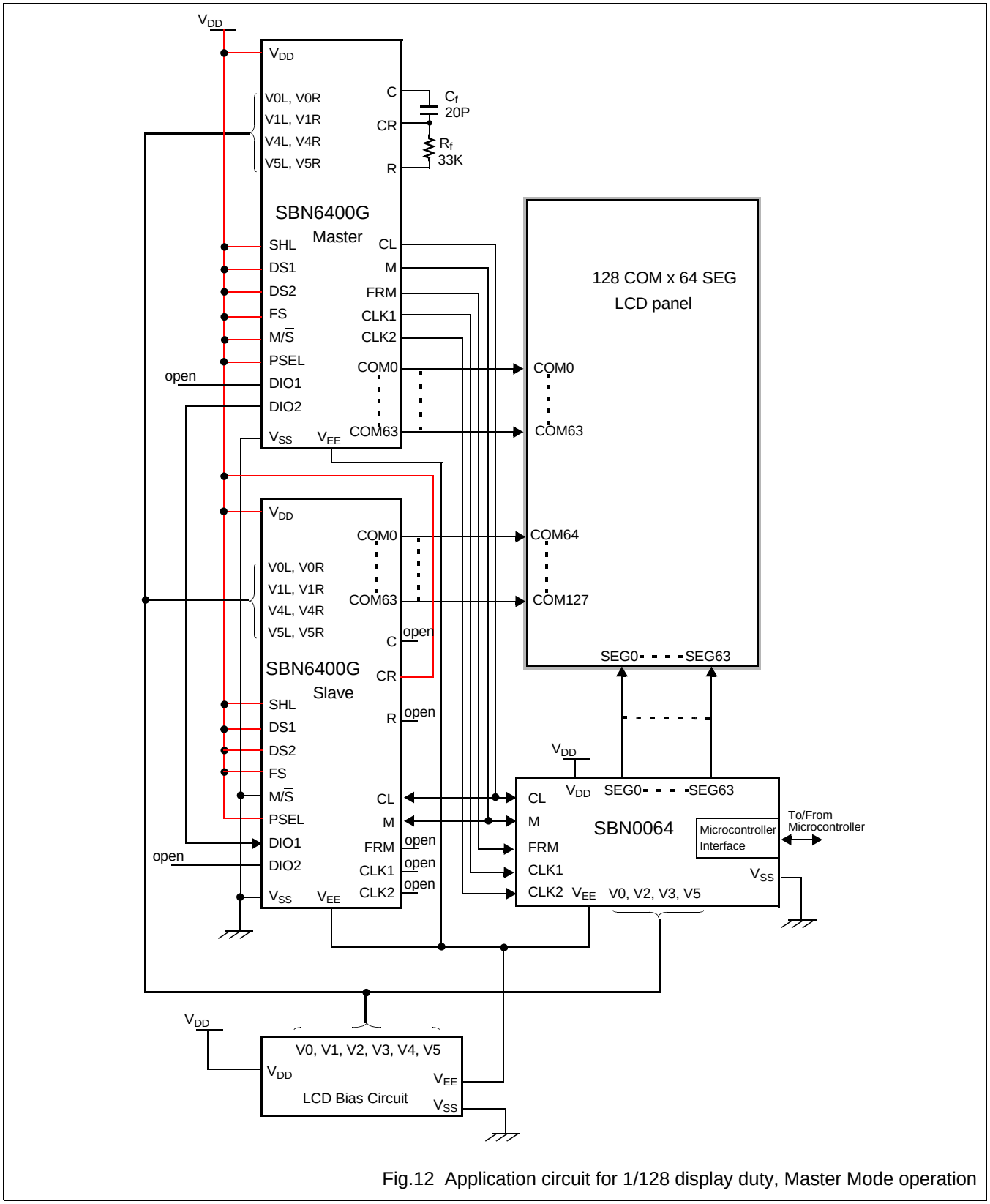


Fig.12 Application circuit for 1/128 display duty, Master Mode operation

8.2 Timing diagram of Master Mode, 1/128 display duty cycle(DS1=H, DS2=H, SHL=H(L), PSEL=H)

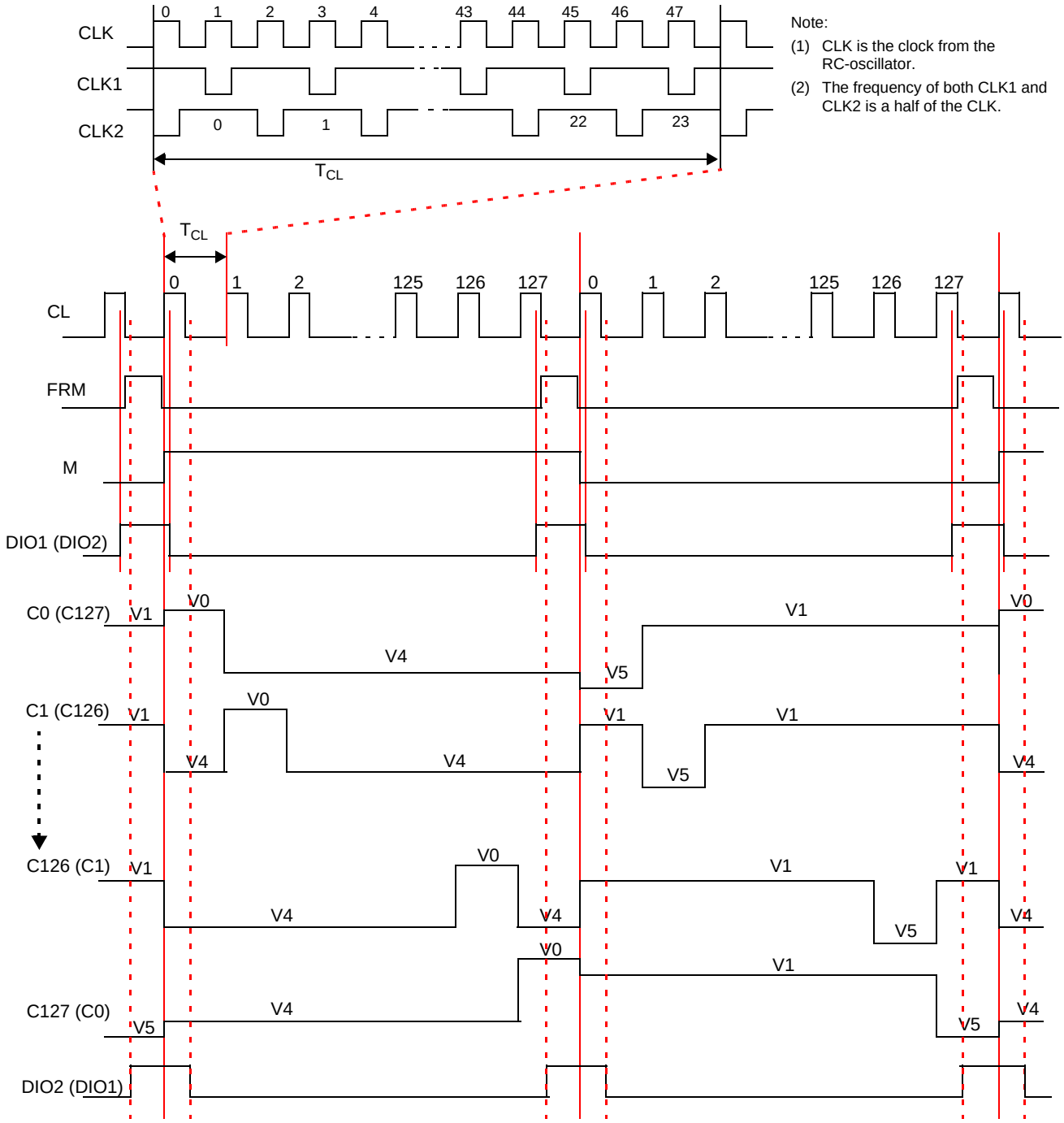


Fig.13 Master mode timing for 1/128 display duty

9 ELECTRICAL CHARACTERISTICS

9.1 Absolute maximum rating

Table 10 Absolute maximum rating

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS}, unless otherwise specified; T_{amb} = −20 to +75 °C

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	voltage on the V_{DD} pin(pad)	−0.3	+7.0	Volts
V_{EE}	Negative voltage on the V_{EE} pin(pad)	V_{DD}-16		Volts
V_{LCD} (note 2)	LCD bias voltage, V_{LCD}=V0-V5		13	Volts
V_I	input voltage on any pin with respect to V_{SS}	−0.3	V_{DD} + 0.3	Volts
P_D	power dissipation		200	mW
T_{stg}	storage temperature range	−55	+125	°C
T_{amb}	operating ambient temperature range	-30	+ 85	°C
Tsol (note 3)	soldering temperature/time at pin		260 °C, 10 Second	

Notes

1. The following applies to the Absolute Maximum Rating:
   a) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.
   b) The SBN6400G includes circuitry specifically designed for the protection of its internal devices from the damaging effect of excessive static charge (ESD). However, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
   c) Parameters are valid over operating temperature range, unless otherwise specified.
   d) All voltages are with respect to V_{SS}, unless otherwise noted.
2. The condition V_{DD}(V0)≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5 must always be met.
3. QFP-type packages are sensitive to moisture of the environment, please check the drypack indicator on the tray package before soldering. Exposure to moisture longer than the rated drypack level may lead to cracking of the plastic package or broken bonding wiring inside the chip.

10 DC CHARACTERISTICS

Table 11 DC Characteristics

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS}, unless otherwise specified; T_{amb} = −20 to +75 °C.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage for logic		4.5	5.0	5.5	V
V_{LCD}	LCD bias voltage V_{LCD}= V0(V_{DD})-V5	Note 1.			13	V
V_{NEG}	V_{NEG}=V_{DD}-V_{EE}				16	V
V_{IL}	LOW level input voltage	Note 2.	0		0.8	V
V_{IH}	HIGH level input voltage	Note 2.	V_{DD}-2.2		V_{DD}	V
V_{OL}	LOW level output voltage of output terminals, at I_{OL}=1.6 mA.	Note 3	0.0		0.3	V
V_{OH}	HIGH level output voltage of output terminals, at I_{OH}=-200μA.	Note 3.	V_{DD} − 0.3		V_{DD}	V
I_{LKG}	Leakage current of input pins(pads)	for all inputs			0.2	μA
I_{STBY}	Standby current at V_{DD}=5 volts	Note 4			3.0	μA
$I_{DD(1)}$	Operating current for master mode with 1/128 display duty cycle	Note 5			960	μA
$I_{DD(2)}$	Operating current for slave mode with 1/128 display duty cycle	Note 6			180	μA
I_{EE}	Operating current measured at the V_{EE} pin(pad)	Note 7			90	μA
C_{in}	Input capacitance of all input pins			5.0	8.0	pF
R_{ON}	LCD driver ON resistance	Note 8			1.5	KΩ

Notes:

1. LCD bias voltage V_{LCD} is V0 - V5. V0 should always be connected to VDD.
2. For all input pins (pads), FS, DS1,DS2, CR, SHL, MS, and PSEL. Also, for all I/Os, DIO1, DIO2, M, and CL when they are used as inputs.
3. For all output pins (pads), CLK1, CLK2, and FRM. Also, for all I/Os, DIO1, DIO2, M, and CL when they are used as outputs
4. Conditions for the measurement: CR=V_{DD}, measured at the V_{DD} pin.
5. This value is measured at the V_{DD} pin (pad). The condition for the measurement is as follows:
   a) R_f=33K, C_f=20 pF,
   b) Display duty cycle=1/128 (DS1=DS2=1),
   c) Master mode (M/$\overline{S}$=1), and FS=SHL=PSEL=1, and
   d) COM0~COM63 were left open.
6. This value is measured at the V_{DD} pin (pad). The condition for the measurement is as follows:
   a) Display duty cycle=1/128 (DS1=DS2=1), Slave mode (M/$\overline{S}$=0), and FS=SHL=PSEL=CR=1,
   b) CL, M, and DIO1 are from the master, and
   c) COM0~COM63 were left open.
7. The condition for the measurement is the same as those described in Note 5, except that the value is measured at the V_{EE} pin(pad).
8. This measurement is for the transmission high-voltage PMOS or NMOS of COM0~COM63. Please refer to Section 12, Pin Circuits, for detailed schematic of these drivers. The measurement is for the case when the voltage differential between the source and the drain of the high voltage PMOS or NMOS is 0.1 volts.

11 AC TIMING CHARACTERISTICS

11.1 CLK1, CLK2 timing for Master Mode

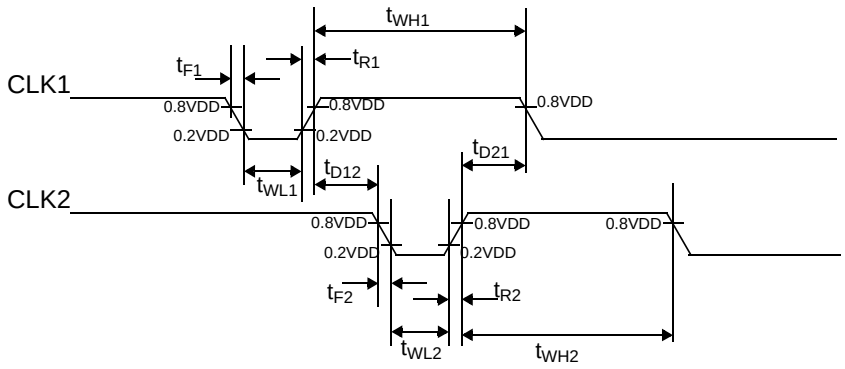


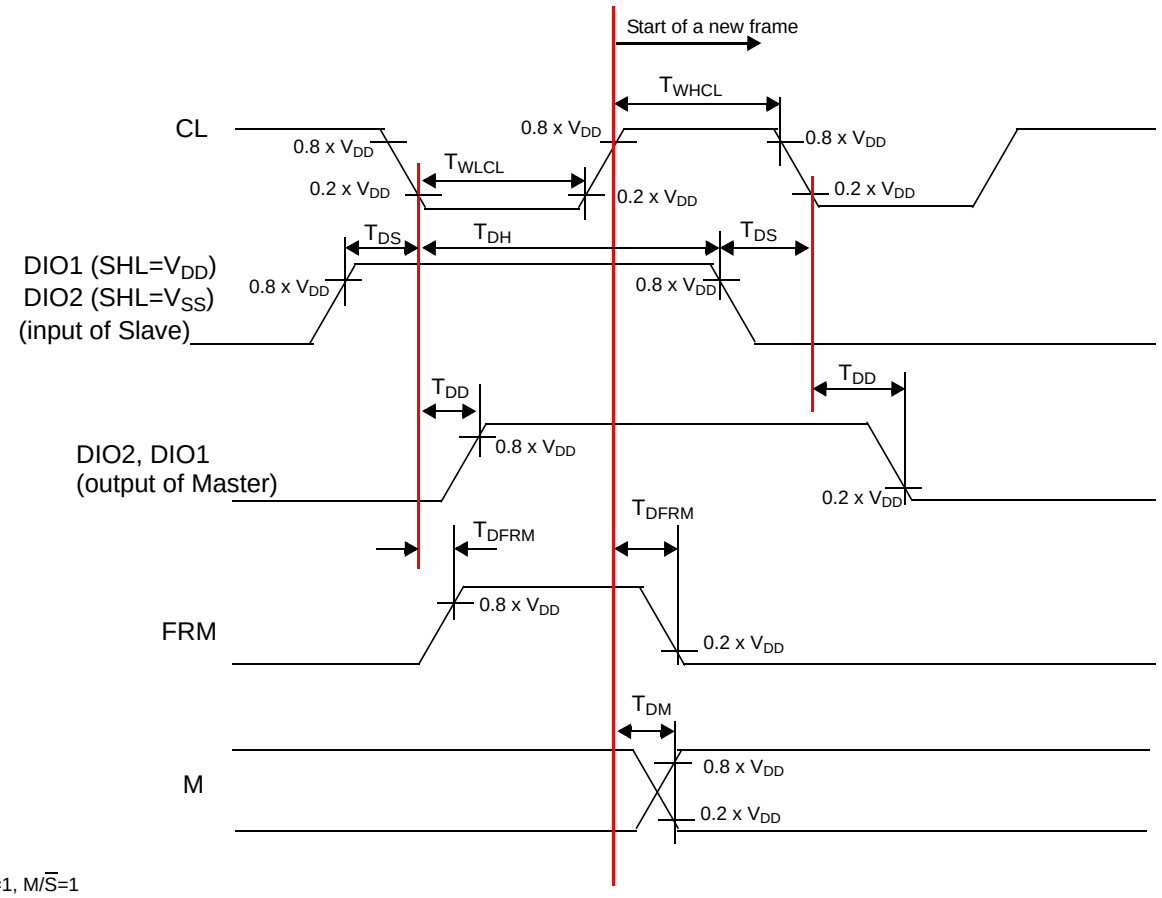
Fig.14 CLK1 and CLK2 timing for Master Mode

Table 12 CLK1 and CLK2 timing characteristics for Master Mode

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified; T_{amb} = −20 to +75 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{WH1}	CLK1 clock high pulse width		2000			ns
T_{WL1}	CLK1 cock low pulse width		600			
T_{R1}	CLK1 clock rise time				130	
T_{F1}	CLK1 clock fall time				130	
T_{WH2}	CLK2 clock high pulse width		2000			
T_{WL2}	CLK2 clock low pulse width		600			
T_{R2}	CLK2 clock rise time				130	
T_{F2}	CLK2 clock fall time				130	
T_{D12}	CLK1-to-CLK2 delay		660			
T_{D21}	CLK2-to-CLK1 delay		660			

11.2 CL, FRM, DIO1, DIO2 and M timing for Master Mode



Note:
(1) PSEL=1, M/$\overline{S}$=1
(2) C_f=20 pF, R_f=33K ohm.

Fig.15 CL, FRM, DIO1, DIO2, and M timing when in Master Mode

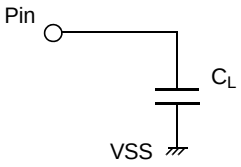
Table 13 CL, FRM, DIO1, DIO2, and M timing for Master Mode

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified; T_{amb} = −20 to +75 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{WHCL}	CL clock high pulse width		33			µs
T_{WLCL}	CL cock low pulse width		33			µs
T_{DS}	DIO1 setup time (for SHL=1), DIO2 setup time (for SHL=0)		18			µs
T_{DH}	DIO1 hold time (for SHL=1), DIO2 hold time (for SHL=0)		38			µs
T_{DD}	Data delay time		4.6			µS
T_{DFRM}	FRM delay time		-1.8		+1.8	µS
T_M	M delay time		-1.8		+1.8	µS

Note:

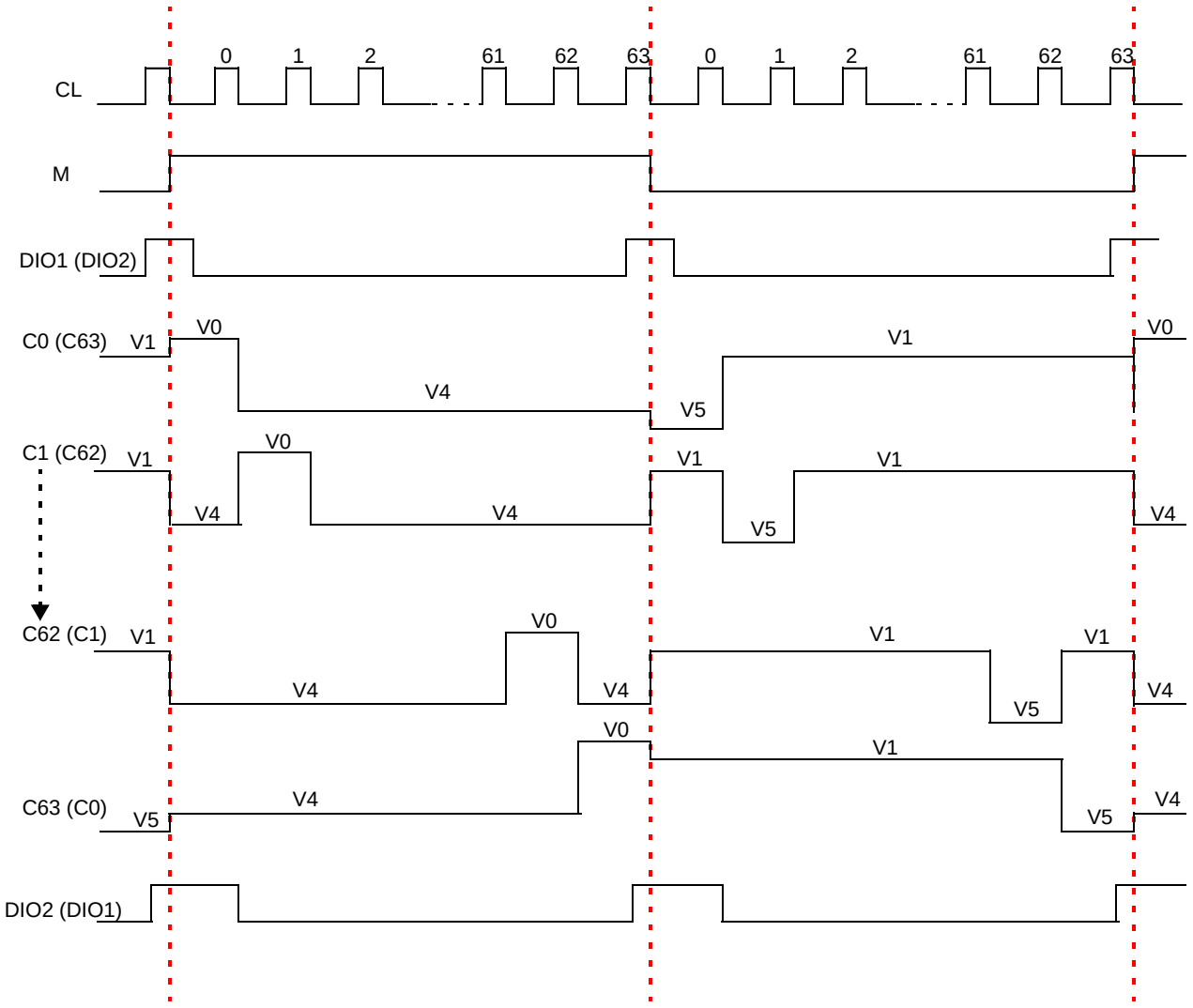
The measurement is with the load circuit connected for output terminals. The load circuit is shown in Fig. 16.



Note:
C_L= 30 pF (including wiring and probe capacitance).

Fig.16 Load circuit for timing diagrams.

11.3 Slave Mode timing for 1/64 display duty cycle(DS1=L, DS2=H, SHL=H(L), PSEL=L)



Note

(1) PSEL=L.

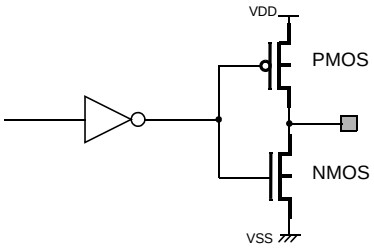
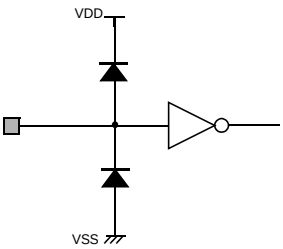
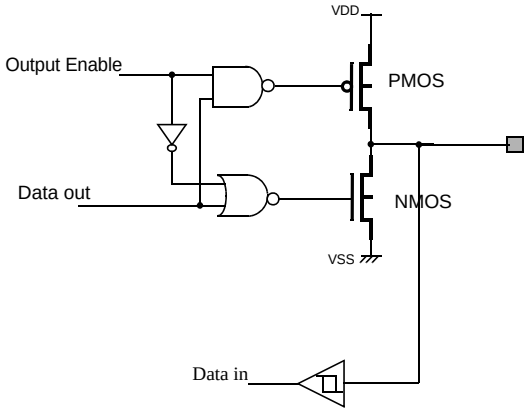
(2) SHL=H.

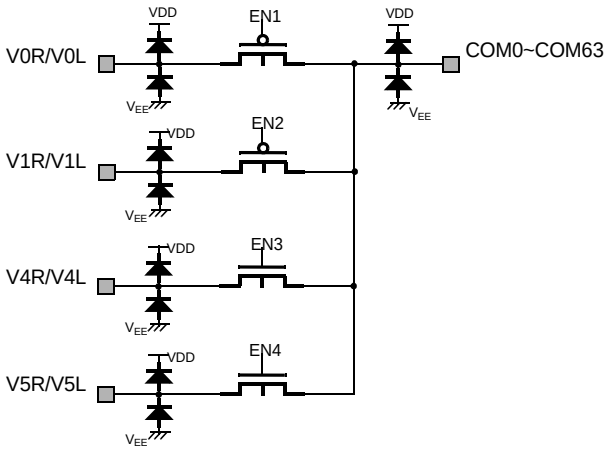
(3) if SHL=L, then COMMON output sequence is inverted, as shown in the parenthesis.

Fig.17 Slave mode timing for 1/64 display duty

12 PIN CIRCUITS

Table 14 MOS-level schematics of all input, output, and I/O pins.

SYMBOL	Input/ output	CIRCUIT	NOTES
CLK1, CLK2, FR	Outputs		The output PMOS and NMOS also act as ESD-protection devices. Their sizes have been enlarged to increase ESD protection voltage.
DS1, DS2, FS, SHL, $\overline{\text{PSEL}}$, M/$\overline{\text{S}}$	Input		
C, R, CR	Inputs	For the pin electronics of the these inputs, please refer to Fig. 5, Section 4.1, On-Chip RC oscillator.	
DIO1, DIO2, M, CL	I/O		The output PMOS and NMOS also act as ESD-protection devices. Their sizes have been enlarged to increase ESD protection voltage.

SYMBOL	Input/ output	CIRCUIT	NOTES
COM0~63, V0R, V0L, V1R, V1L, V4R, V4L, V5R, V5L			

13 APPLICATION NOTES

1. It is recommended that the following power-up sequence be followed to ensure reliable operation of your display system. As the ICs are fabricated in CMOS and there is intrinsic latch-up problem associated with any CMOS devices, proper power-up sequence can reduce the danger of triggering latch-up. When powering up the system, control logic power must be powered on first. When powering down the system, control logic must be shut off later than or at the same time with the LCD bias (V_{EE}).

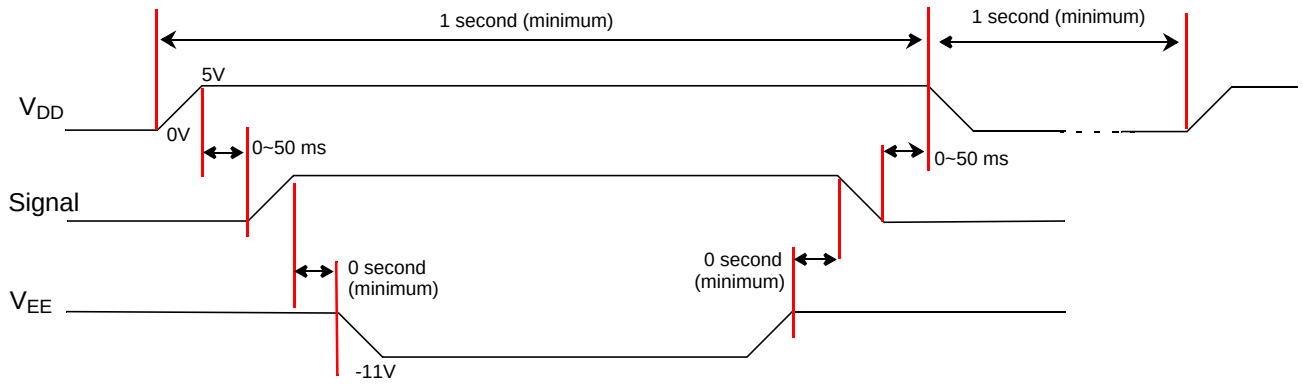


Fig.18 Recommended power up/down sequence

2. The metal frame of the LCD panel should be grounded.
3. A 0.1 μF ceramic capacitor should be connected between V_{DD} and V_{SS}.
4. A 0.1 μF ceramic capacitor should be connected between V_{DD} (or V_{SS}) and each of V1, V2, V3, V4, and V5.

14 PACKAGE INFORMATION

Package information is provided in another document. Please contact Avant Electronics for package information.

15 SOLDERING

15.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. For more in-depth account of soldering ICs, please refer to dedicated reference materials.

15.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, please contact Avant for drypack information.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

15.3 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Repairing soldered joints

Fix the component by first soldering two diagonally- opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

16 LIFE SUPPORT APPLICATIONS

Avant's products, unless specifically specified, are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Avant customers using or selling Avant's products for use in such applications do so at their own risk and agree to fully indemnify Avant for any damages resulting from such improper use or sale.